可测性设计（DFT）基本知识及流程介绍

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Agenda

1. Manufacturing Defect
2. Manufacturing Testing
3. What is DFT and Why DFT
4. Describe Different DFT Techniques
5. DFT Flow Introduce

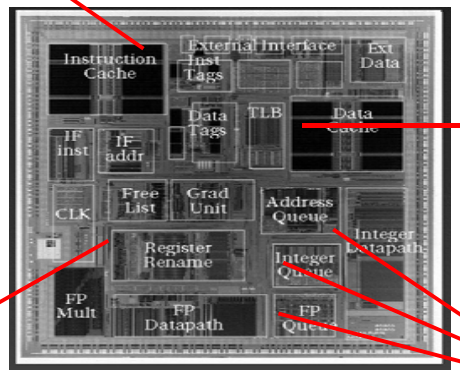
What Is a Manufacturing Defect?

- Physical Defect:

  A on-chip **flaw** introduced during fabrication or packaging of an individual ASIC that makes the device **malfunction**.

Common Physical Defects

Short Circuit

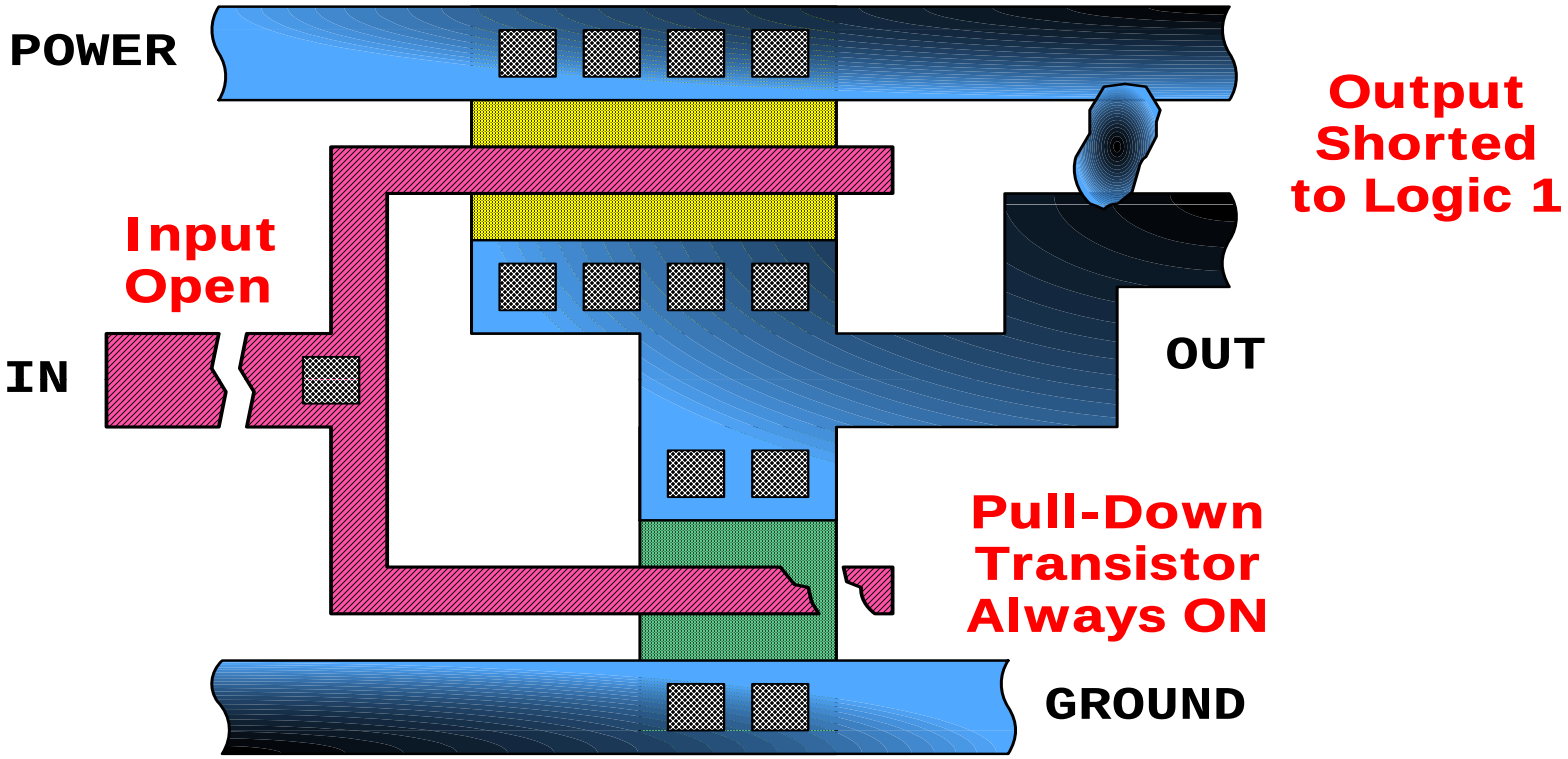


Open Circuit

Transistor Always ON

Oxide Pinholes

Physical Defects in CMOS

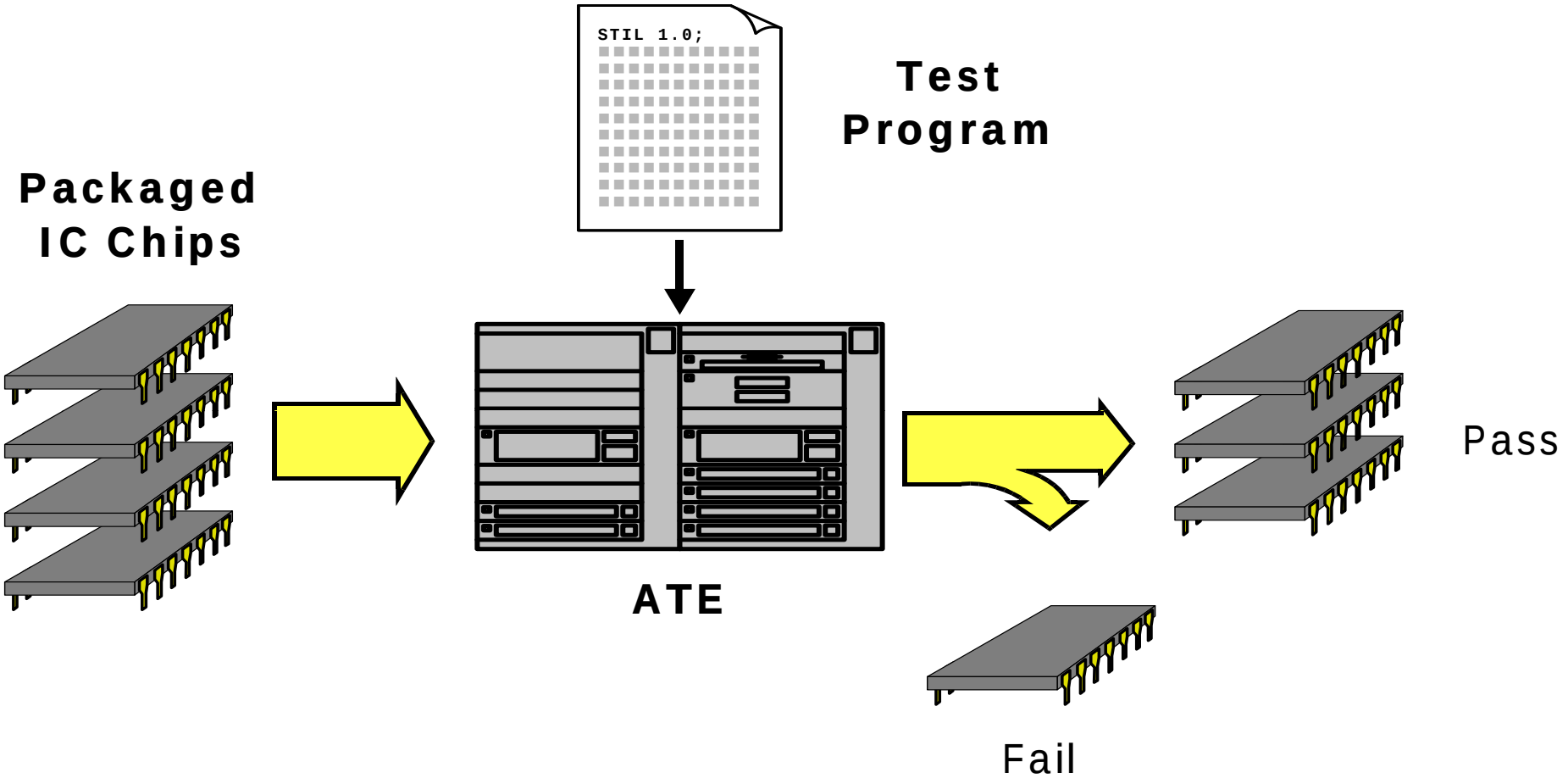


Manufacturing Test

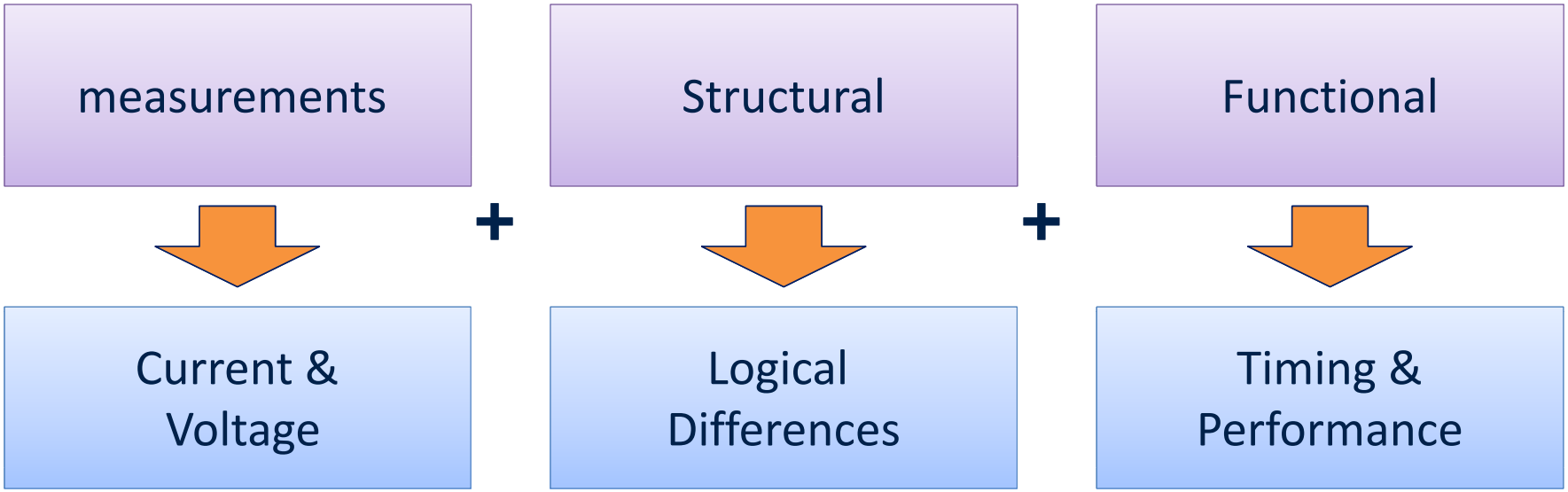
- There is no perfect IC fabrication process! Physical defects may exist within the manufactured chip.

- A defect may cause a logical fault , or changes the parametric properties of the IC and/or negatively affects the product’s reliability.

Manufacturing Test(cont)



Manufacturing Test(cont)



Test Automation

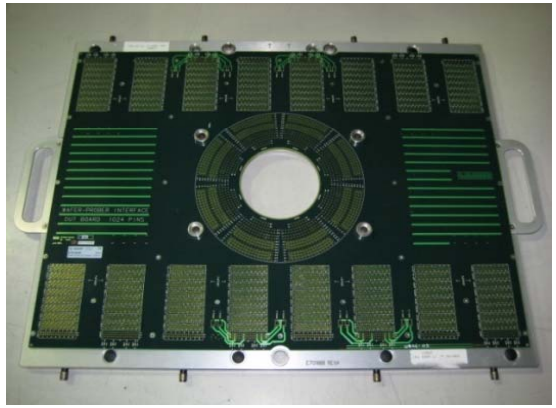
Test Automation

- Automated Test Equipment is essential part of manufacturing
- Highly automated throughput-oriented equipment
- Investment > 1M$ per system
- Multiple systems at each manufacturing site

ATE Example: Agilent 93000

ATE Example: Agilent 93000 (cont)

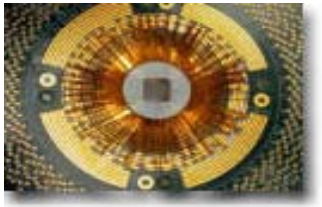
- Workstation
  - Test software, interface and control of mainframe
  - Test engineer computer



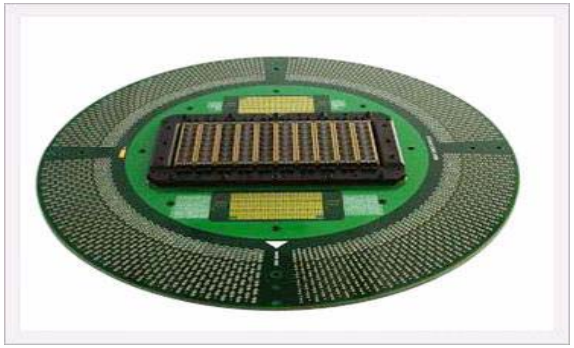
- Mainframe
  - Test computer
  - Power sources
  - Measurement instruments

- Testhead
  - Device Interface Board (DIB) to DUT
  - Sensible measurement equipment kept close to DUT

Probers



Probecard



- Robotic machine that manipulates the wafers
- Connects individual chip to probe card needles
- ATE is connected for measurement

Manufacturing Test(cont)

- A speck of dust on a wafer is sufficient to kill chip
- Manufacturing testers are very expensive
  - Think about it at beginning phase, careful plan about chip performance requirment, ATE, Load Board..
  - DFT designer pay attention to it during dft implement, such as chain length, memory instance number per test step
  - ATPG efficiency
  - selection of test vectors

Agenda

1	Manufacturing Defect
2	Manufacturing Testing
3	What is DFT and Why DFT
4	Describe Different DFT Techniques
5	DFT Flow Introduce

Test Definition

Test

- checking a manufactured object for matching with a set of specified properties.

Test Spec

- A set of product features and related check rules required to guarantee product quality and product reliability.

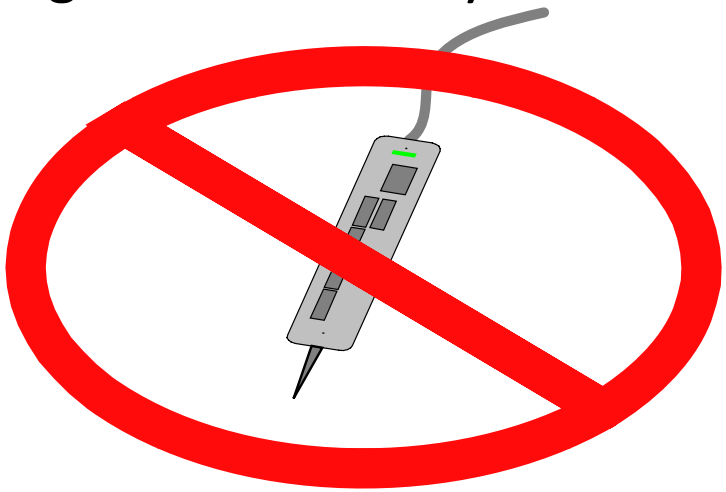
Testability

- the effort for test development and test application.

Rules for Detecting Faults

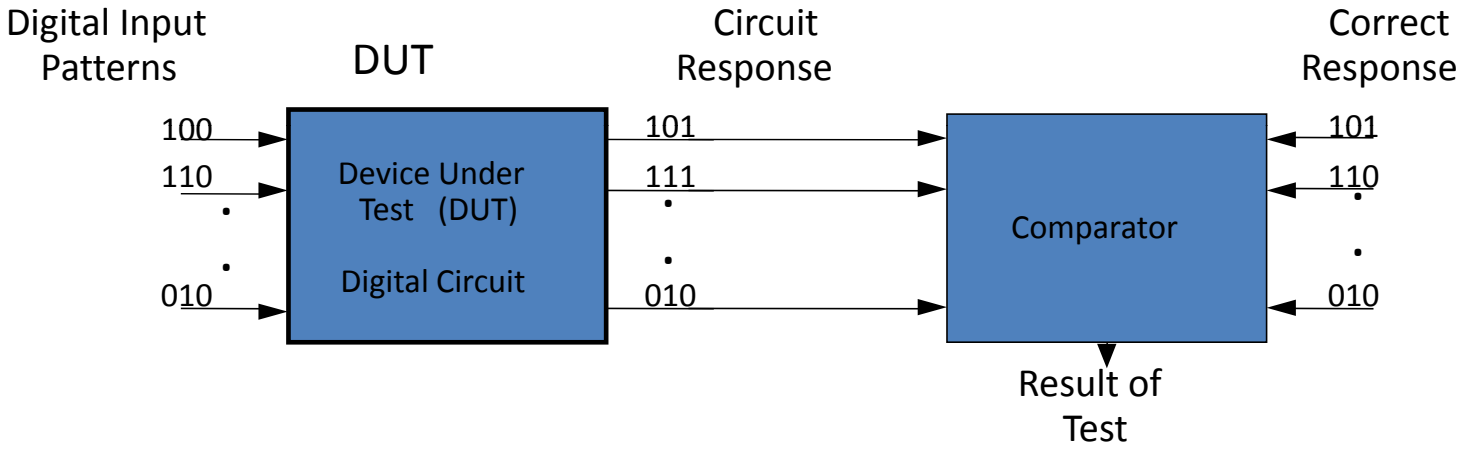
- Rules of the Game:

  Tester access to the DUT is **only** allowed through its **primary** I/O ports because Internal Probing of IC Too Costly!



Way of Chips to be Tested

- The internals of the integrated circuit is not accessible.
  - test vectors are applied to the inputs
  - Outputs are compared to expected values
  - Process is automatized using an ATE

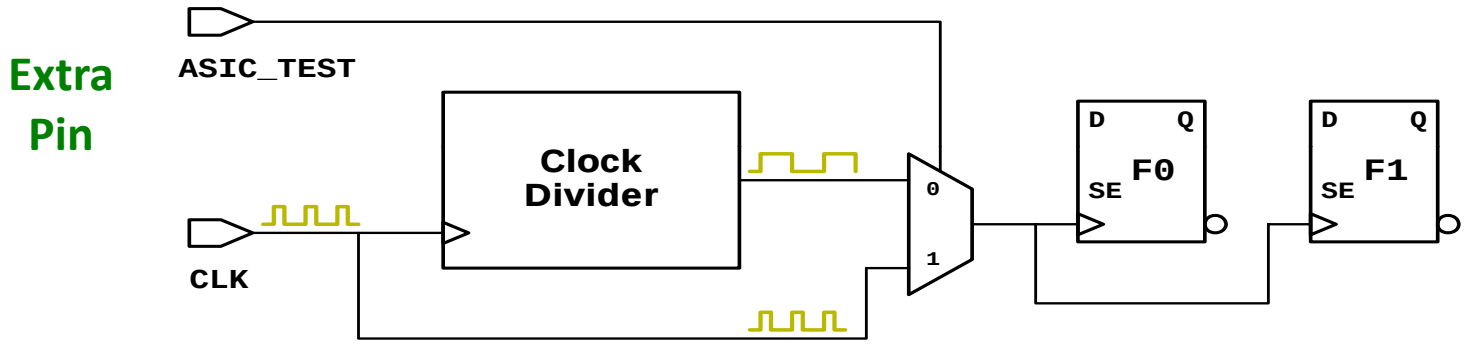


Design For Test

- DFT refers to those design techniques that
  - Make test generation and test application cost-effective
  - Make extra design effort in making an IC testable
  - Involve inserting or modifying logic, and adding pins
  - Help design the chip to increase observability and controllability
- If each register could be observed and controlled, test problem reduces to testing combinational logic between registers
- Logic blocks could enter test mode where they generate test patterns and report the results automatically.

What is Design-for-Testability?

- Design for Testability (DFT):
- Extra design effort invested in making an IC testable
- Involves inserting or modifying logic, and adding pins



Typical DFT Hardware

Observability and Controllability

- Observability: ease of observing a node by watching external output pins of the chip
- Controllability: ease of forcing a node to 0 or 1 by driving input pins of the chip
- Combinational logic is usually easy to observe and control

Roles of Testing

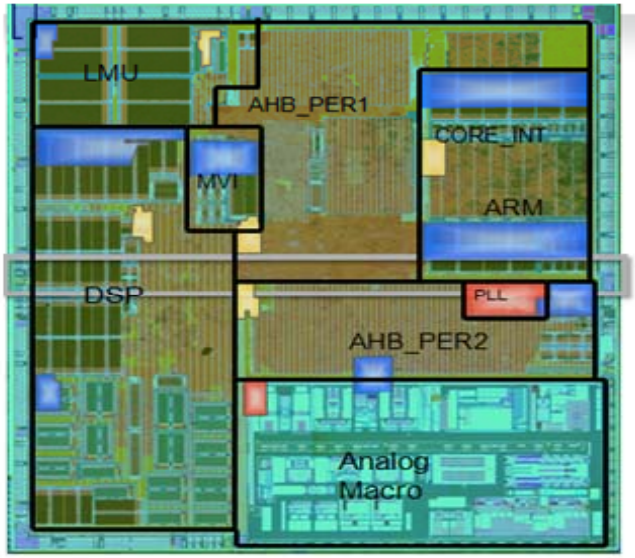
- Detection: determination whether or not the (DUT) has faults
  - Identification of process flow
  - Detection of chips that must not be sold to customers
- Diagnosis: location and identification of a specific fault
- Device characterization
- Failure mode analysis (FMA): determination of manufacturing process issues that may have caused defects on the DUT
  - manufacturing process improve and the yield improve

Real Tests

- Based on analyzable fault models which may not perfectly match real defects
- Incomplete test coverage due to the extreme complexity of IC
    - Mixed-mode analog and digital
    - Several cores, memory
    - Hundreds of millions of transistors
- Some good chips are rejected (yield loss).
- Some bad chips pass tests (defect level).

What we test by DFT

众所周知，芯片主要由三大部分构成.
芯片示例-可见下图



Test of Digital Standard Logic
- Fault Models and Fault Simulation
- Scan Synthesis and ATPG
- Advanced Scan Test Architectures
- Built-In Self Test
- Test Concept Engineering

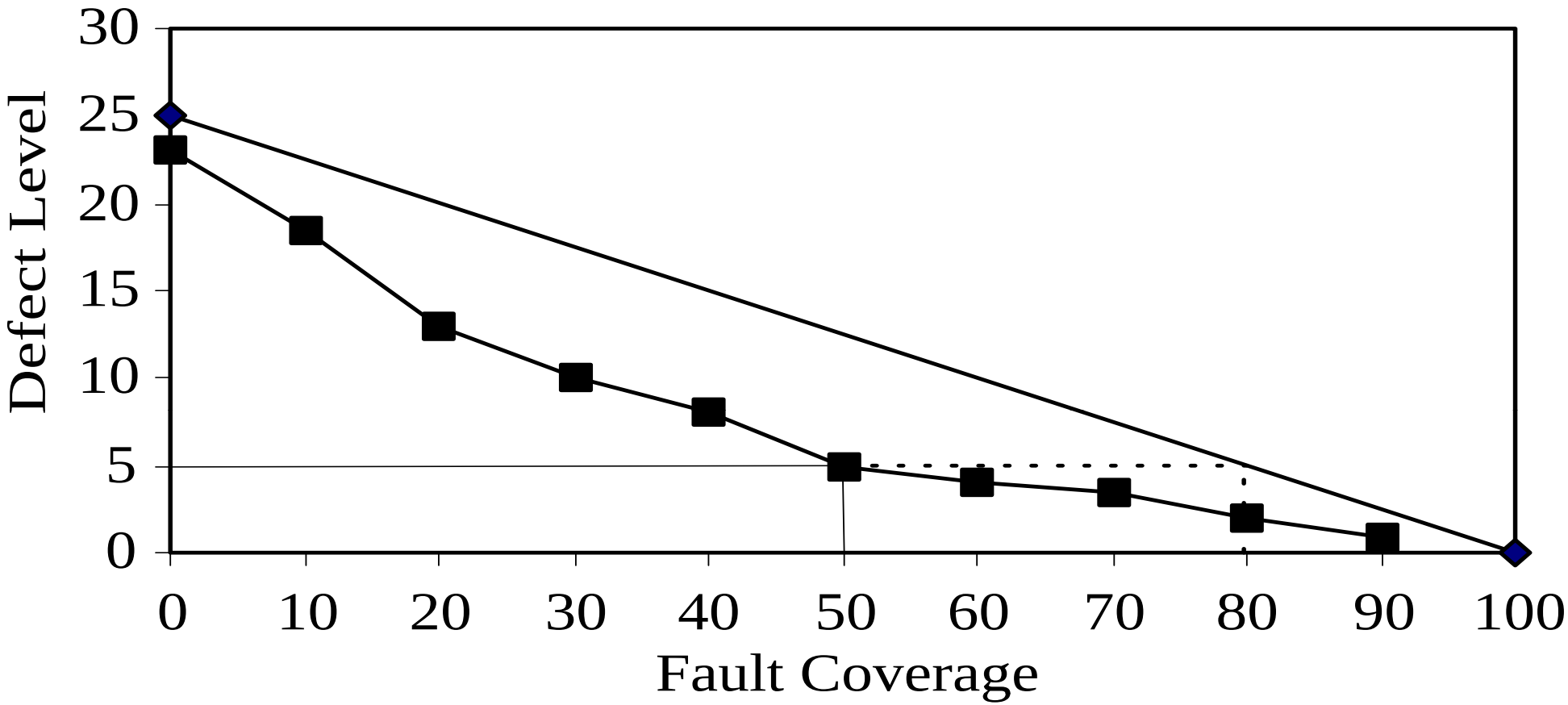
Test of SRAMs and ROMs
- Memory Test

Test of IO Logic
- Boundary Scan Test & Test Control

1 与电路板和其他芯片的接口-IO pad
2 存放程序的空间-ram 和 rom
3 搭建逻辑电路的基本组件 –标准逻辑单元

我们 DFT 工程师所有的工作的目的只有一个-设计和插入数字电路，测试整个芯片的制造质量，筛选出没有制造缺陷的芯片。

Defect Level vs Fault Coverage



DFT Cost

- DFT cost
  - Area cost；
  - Performance penalty ；
- ATPG tool cost and pattern debug cost
- ATE testing cost

DFT Cost (cont)

- Test cost reduce
  - Proper test plan, such as chain length, memory concurrent testing…;
  - Reduce pattern number;
  - Increace test frequency;

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DFT Methods

- No single methodology solves all testing problems.
- No single DFT techniqne is effective for all kinds of circuits.

DFT Methods(cont)

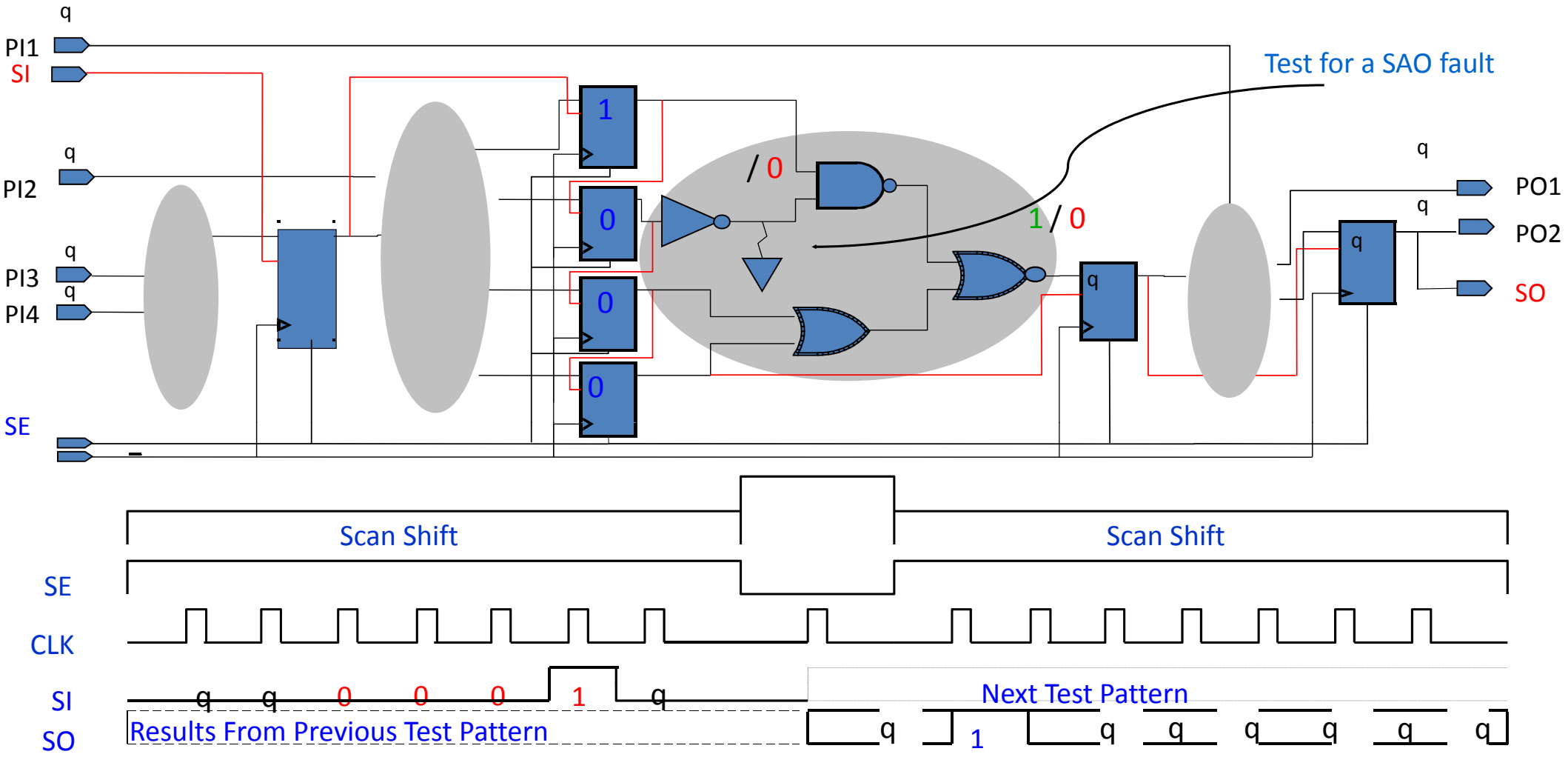
- Ad-hoc
- Structured
  - Scan
  - Built-in self-test (BIST)
  - Boundary scan

Scan

- To provide controllability and observability of internal state variables for testing

- To turn the sequential test problem into a combinational one

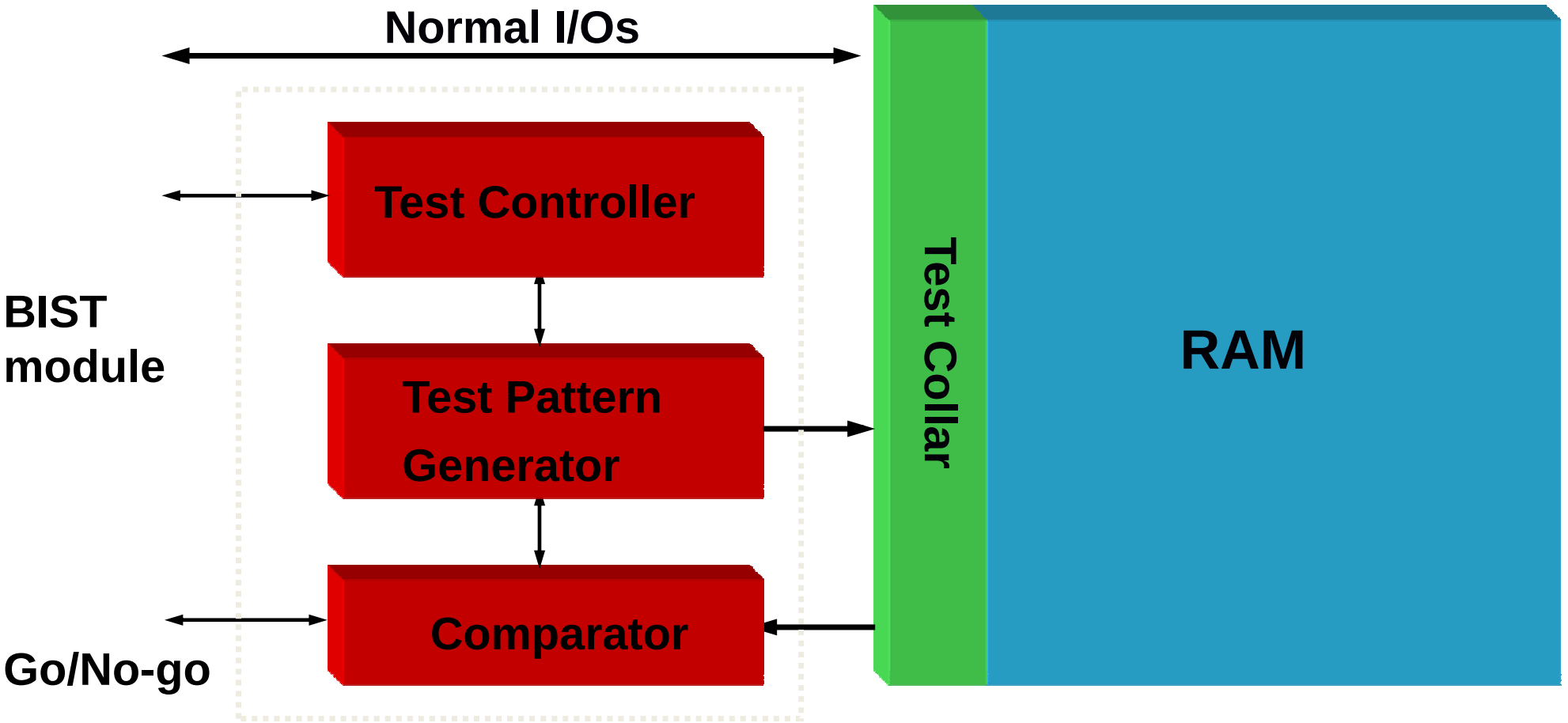
Scan(cont)


PI1
SI
PI2
PI3
PI4
SE
q
1
0
0
0
/ 0
1 / 0
Test for a SAO fault
PO1
PO2
SO
Scan Shift
Scan Shift
SE
CLK
SI
SO
q q 0 0 0 1 q
Results From Previous Test Pattern
Next Test Pattern
q 1 q q q q q

Advantages/Disadvanges

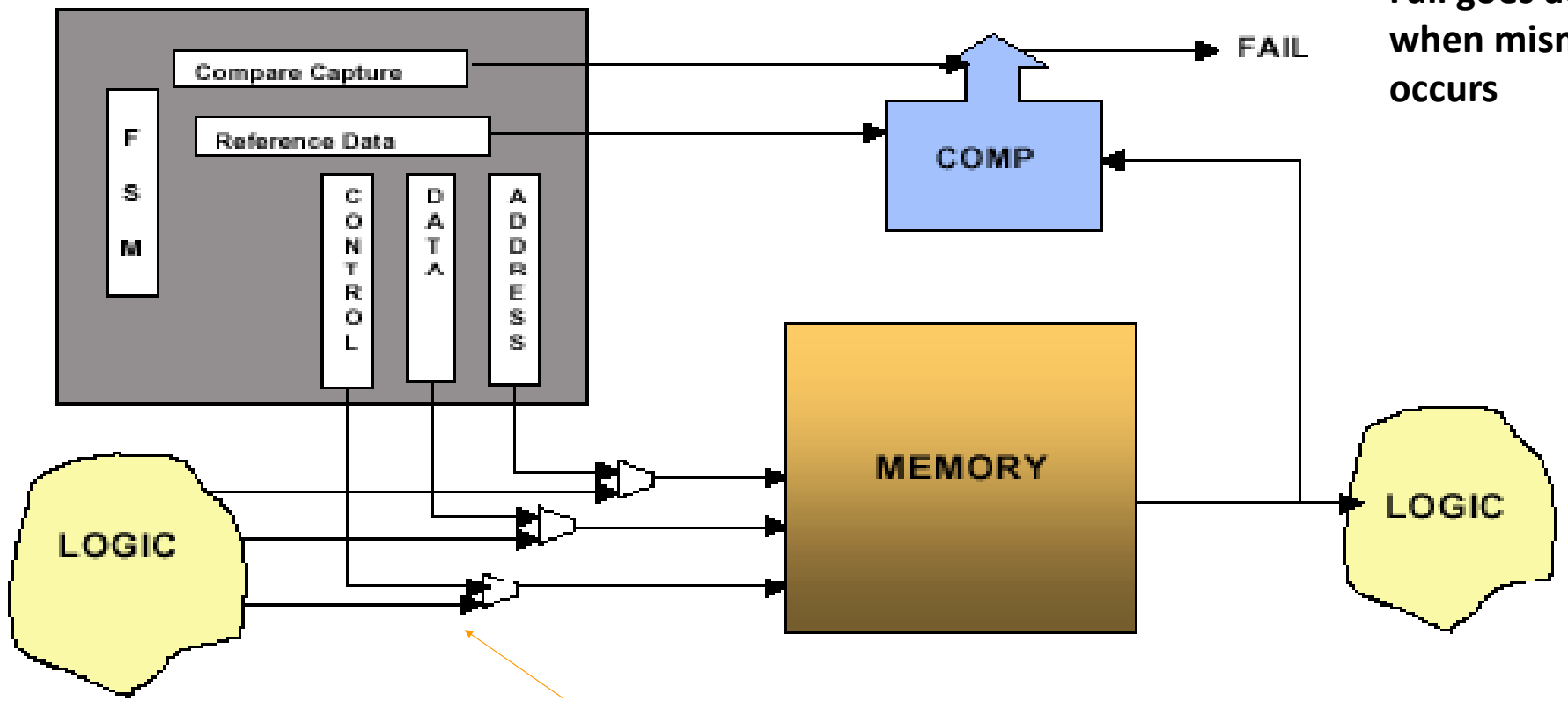
- Advantages
  - Design automation, Automated DFT hardware insertion Combinational ATPG
  - High fault coverage
  - Reasonable area (~15%) and speed (~5%) overhead
- Disadvantages
  - Large test data volume and long test time
  - A slow speed test

Typical Memory BIST Architecture



MBIST Without Diagnosis Architecture

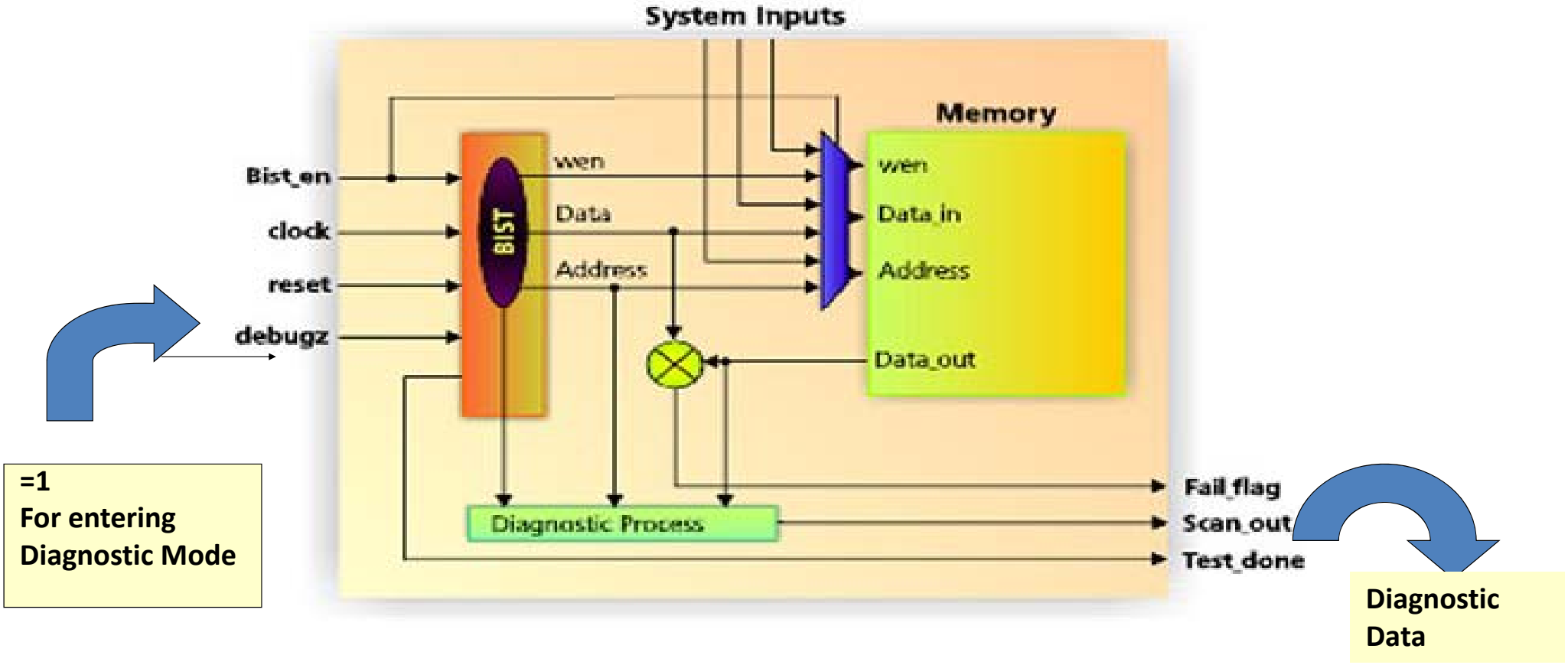
BIST controller creates and applies patterns



Fail goes active when mismatch occurs

Multiplexers select b/w system and test data

BIST with Diagnostic Block



Boundary Scan

Motivation and benefits:

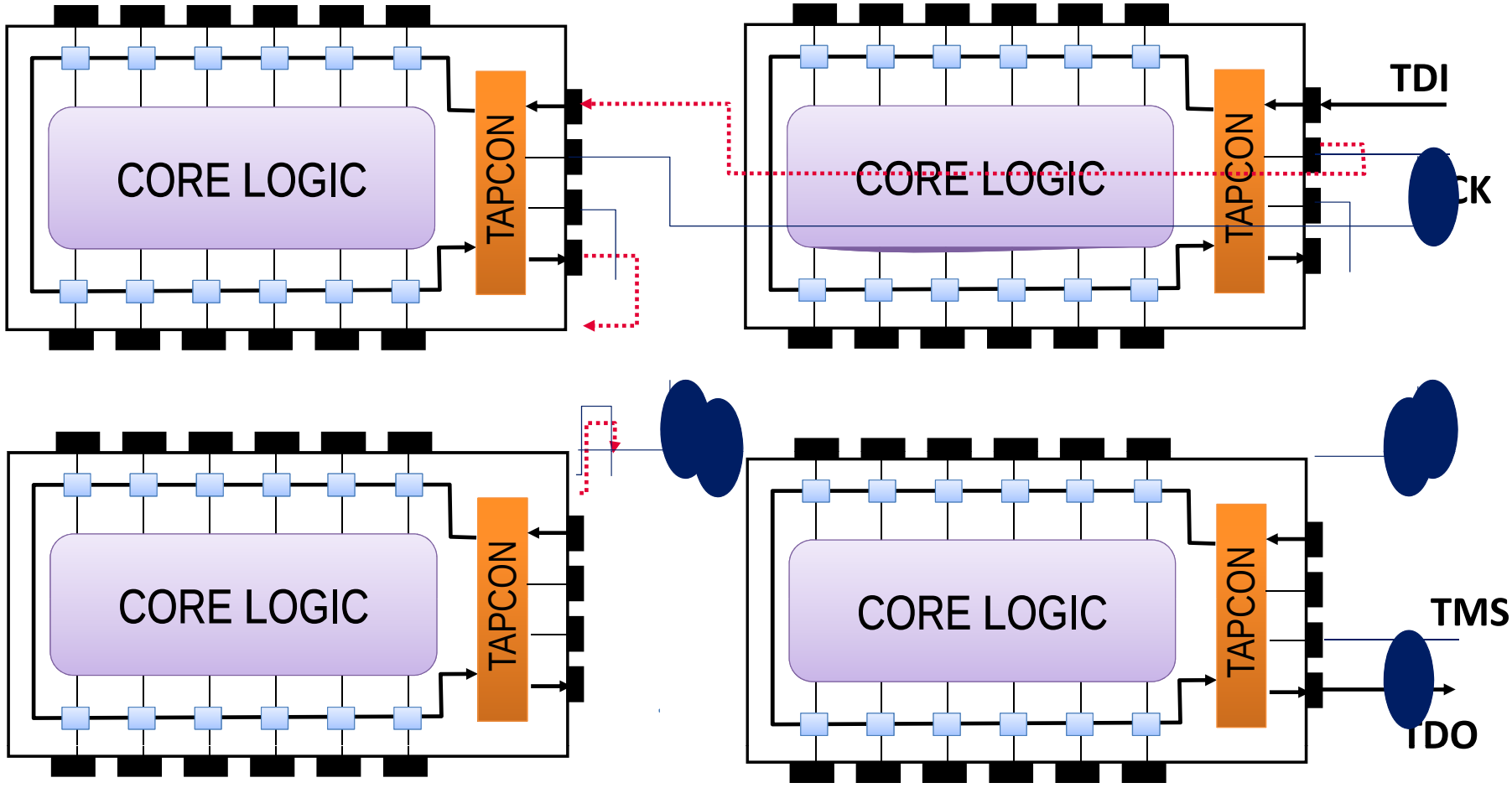
1.Detect board manufacturing process faults, including wrong/missing components, pin stuck/short/open, assist interconnection test on the board-level

2. A many degrees of freedom are allowed

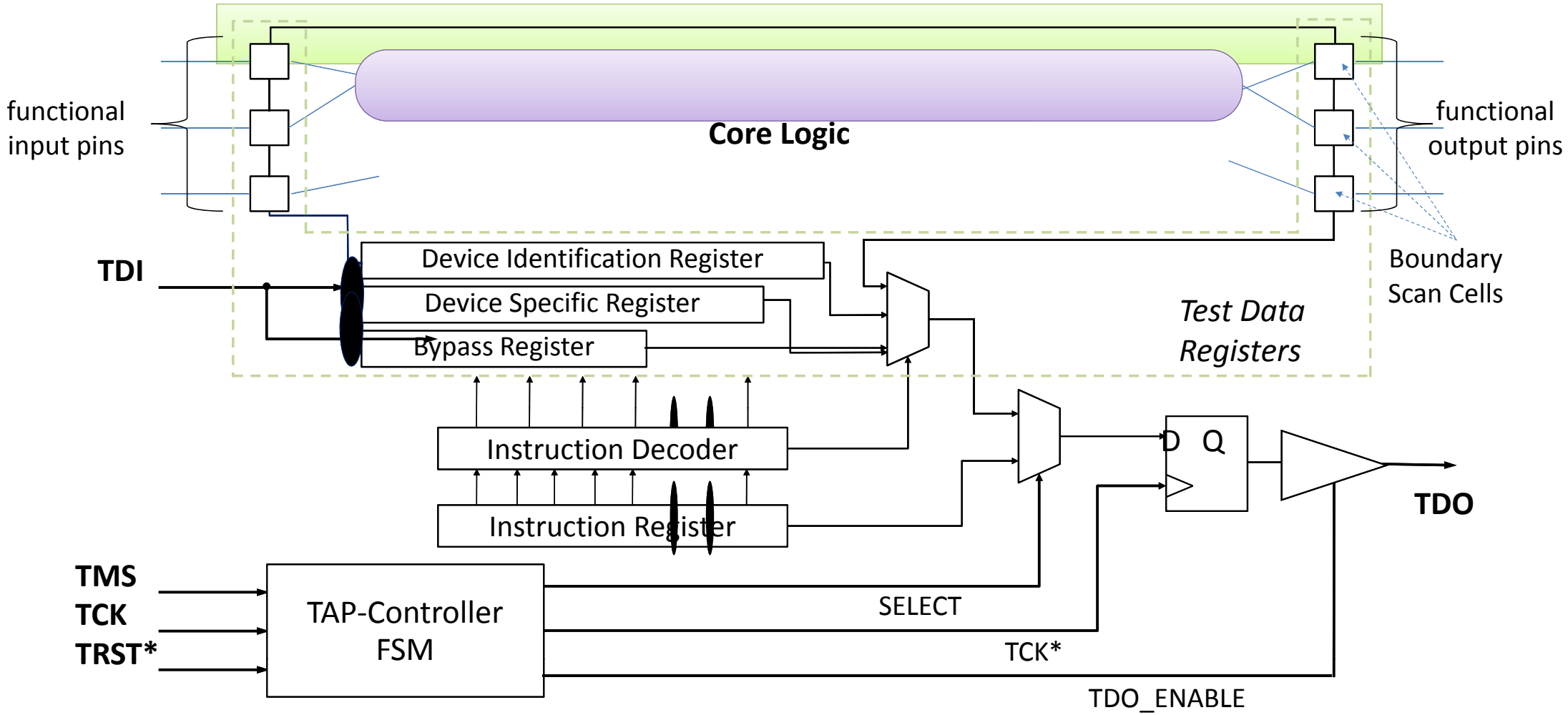
Specification

- Independent sub-system (independent clocks)
- Pins: TDI, TDO, TMS, TCK are mandatory
- Reset: optional TRST* pin or power-on reset circuitry
- Registers:
  - Instruction, bypass, boundary-scan (mandatory)
  - Device identification, design-specific data (optional)
- BSDL (boundary-scan description language)

Board Test Example



JTAG Architecture



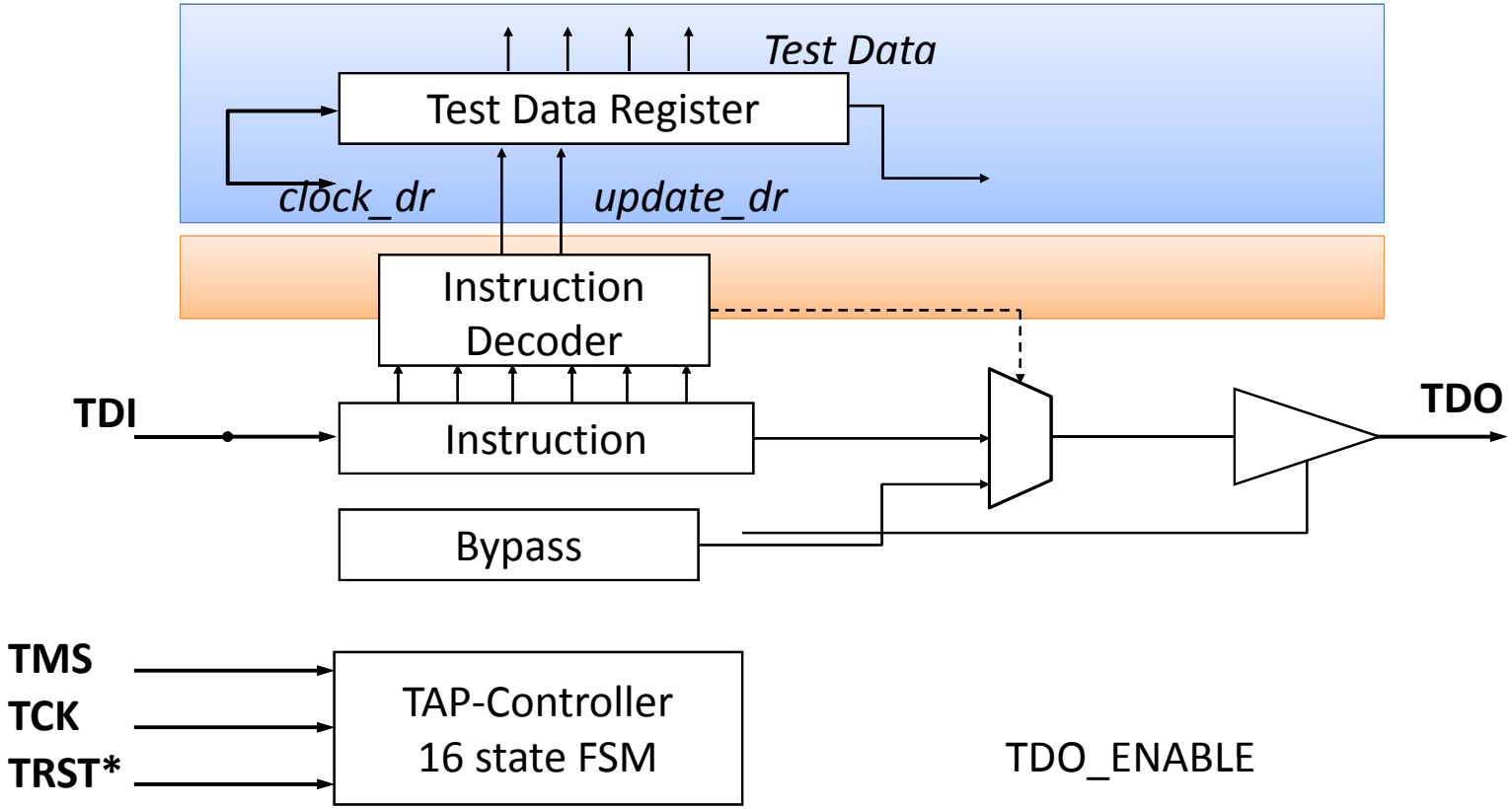
Instructions (1)

- BYPASS (mandatory)
  - Provides a minimum length serial shift register from TDI to TDO
- SAMPLE/PRELOAD (mandatory)
  - Allows a snapshot of all I/O lines
  - For loading the BSR serially
- EXTEST (mandatory)
  - Data shifted into the BSR will be available at the chip outputs
- INTEST
  - Data shifted into the BSR is driven on the core logic inputs

Instructions (2)

- IDCODE (mandatory, if ID register available)
  - ID register selected for reading HW identification
- CLAMP
  - Holds the chip outputs at values shifted in before, while bypass register is active
- HIGHZ
  - All chip outputs are placed in high impedance state
- User-defined test mode
  - May be private or public

User-Defined Instru/Data Register



TAP-Controller accesses external register

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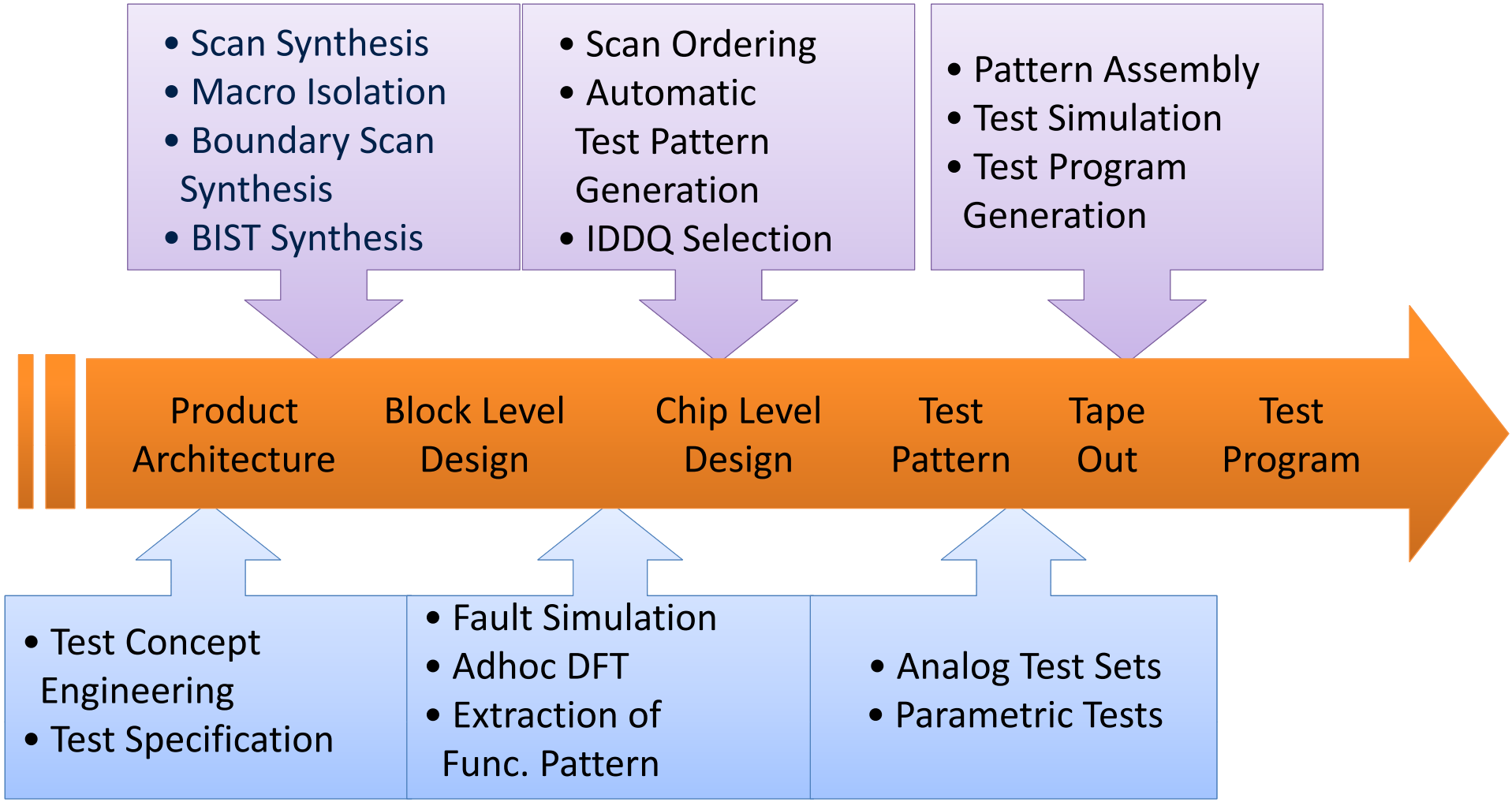
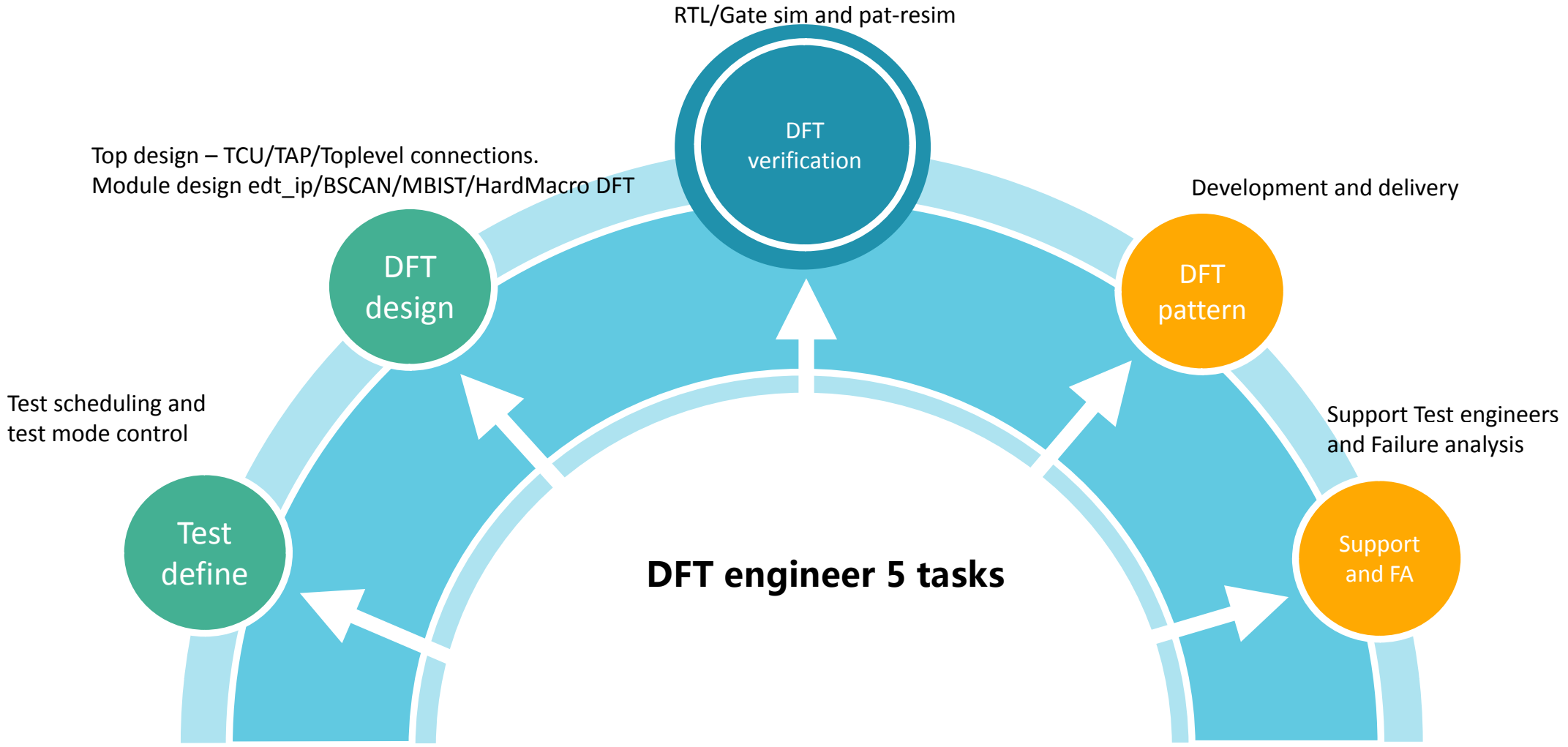
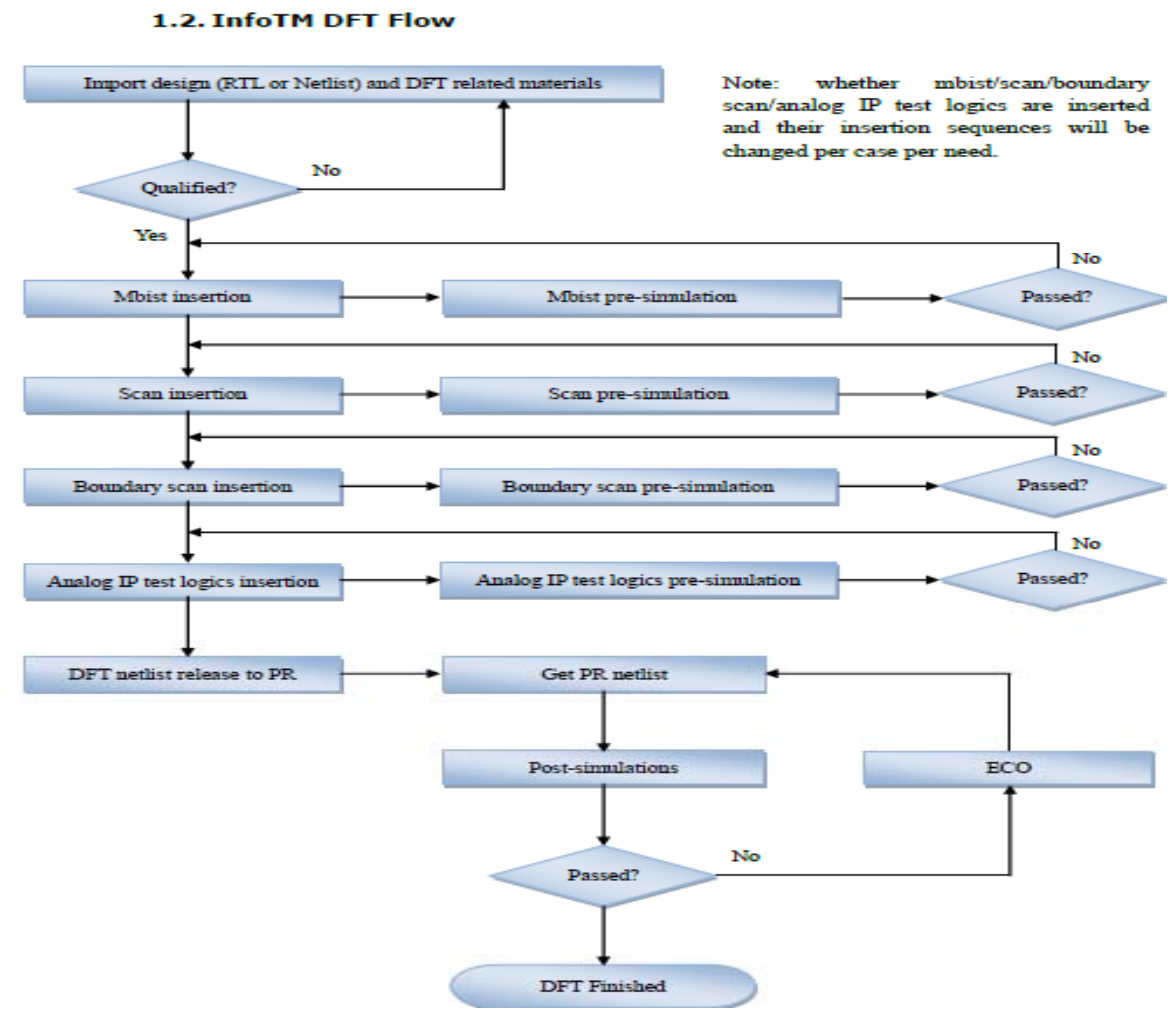
Test Development Flow



DFT engineer 5 tasks



DFT Flow (top)


1.2. InfoTM DFT Flow
Import design (RTL or Netlist) and DFT related materials
Qualified?
No
Yes
Note: whether mbist/scan/boundary scan/analog IP test logics are inserted and their insertion sequences will be changed per case per need.
Mbist insertion
Mbist pre-simulation
Passed?
No
Scan insertion
Scan pre-simulation
Passed?
No
Boundary scan insertion
Boundary scan pre-simulation
Passed?
No
Analog IP test logics insertion
Analog IP test logics pre-simulation
Passed?
No
DFT netlist release to PR
Get PR netlist
Post-simulations
ECO
Passed?
No
DFT Finished

DFT flow inputs/outputs

	Test Development Flow			
	Phase	**DFT Team Task**	**Need inputs**	**Send outputs**
1	Product Architecture	Test concept defined – test scheduling and test mode control	Chip test requirements/concepts	Test Specification
2	Block Level Design	DFT design -insert scan/edt_ip/MBIST/HardMacro DFT DFT verification - RTL/Gatelevel sim (block_level)	Block level RTL/netlist/sdc/lib	Block level RTL/netlist/sdc (add DFT)
3	Chip Level Design	DFT design -TCU/TAP/adhoc-DFT/BSCAN/Toplevel connections DFT verification - RTL/Gatelevel sim (chip_level)	Top level RTL/netlist/sdc/lib	Top level netlist/sdc (add DFT)
4	Test Pattern Generate	DFT Patterns - Development (Func pat/ATPG/IDDQ/Analog Test Sets/Parametric Tests)	Top level PR netlist/sdc/lib	Test patterns (meet with coverage requirments)
5	Tape Out	DFT Patterns - Delivery (Func pat/ATPG/IDDQ/Analog Test ets/Parametric Tests) DFT verification - Patterns gatelevel sim (chip_level max/min)	Top level PR netlist/sdc/lib/SDF	1 Simulation max/min clean 2 Final test patterns (wgl/evcd files...) 3 Final Test Specification and Patterns Guideline
6	Test Program	Support Test engineers and Failure analysis	Tester logs ...	Test reports/Debug reports/Test seq

DFT flow used tools

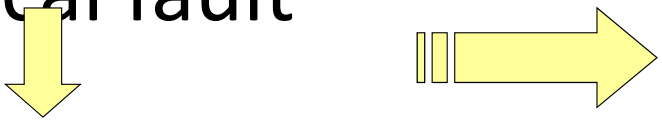
DFT Tools		
Phase		**Need Tools**
1	Insert scan chains	Design Compiler/Tessent
2	Insert edt/compress ip	Tessent - TestKompress/TMAX
3	Insert MBIST	Tessent MBIST/MBIST Architect
4	Insert BSCAN	Tessent BSCAN / BSCAN Architect
5	Test Pattern Generate	Tessent - TestKompress/TMAX
6	Test scan Diagnose	Tessent - Diagnosis
7	Simulation	VCS

Backup

电　　话：86-21-50277721　　业务 邮箱：sales@infotmic.com.cn　　技术 支持：support@infotmic.com.cn

Fault Modeling

Physical fault

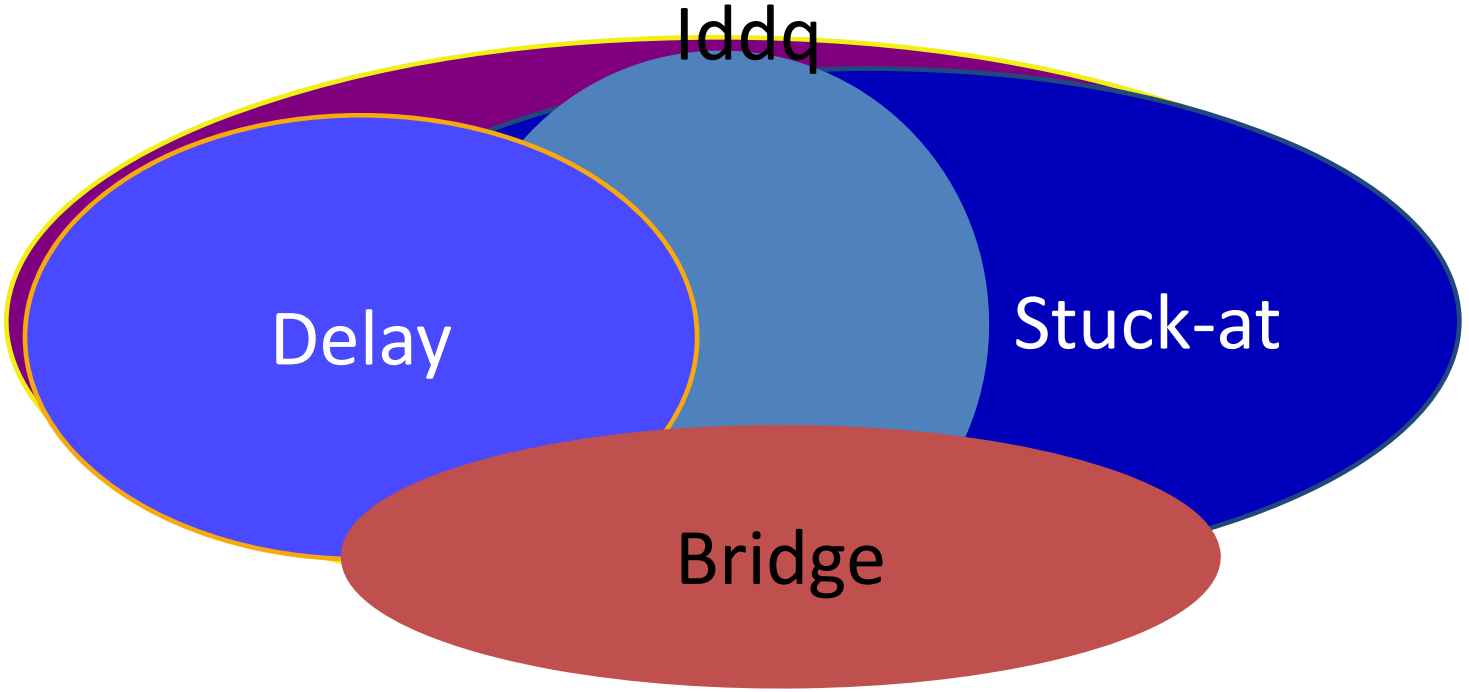


Logic fault

IO leakage or short between
net open
material pollution
electronic migration
metal stress
…
…

signal hard fault
delay fault
static current fault
…
…

Fault Modeling



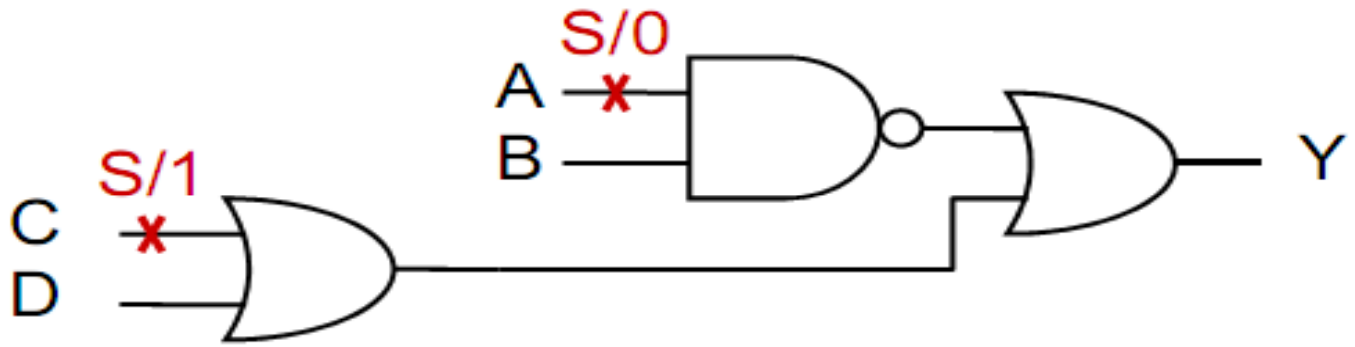
Fault model **:**

A logical model representing the effects of a physical defect

Fault Modeling(cont)

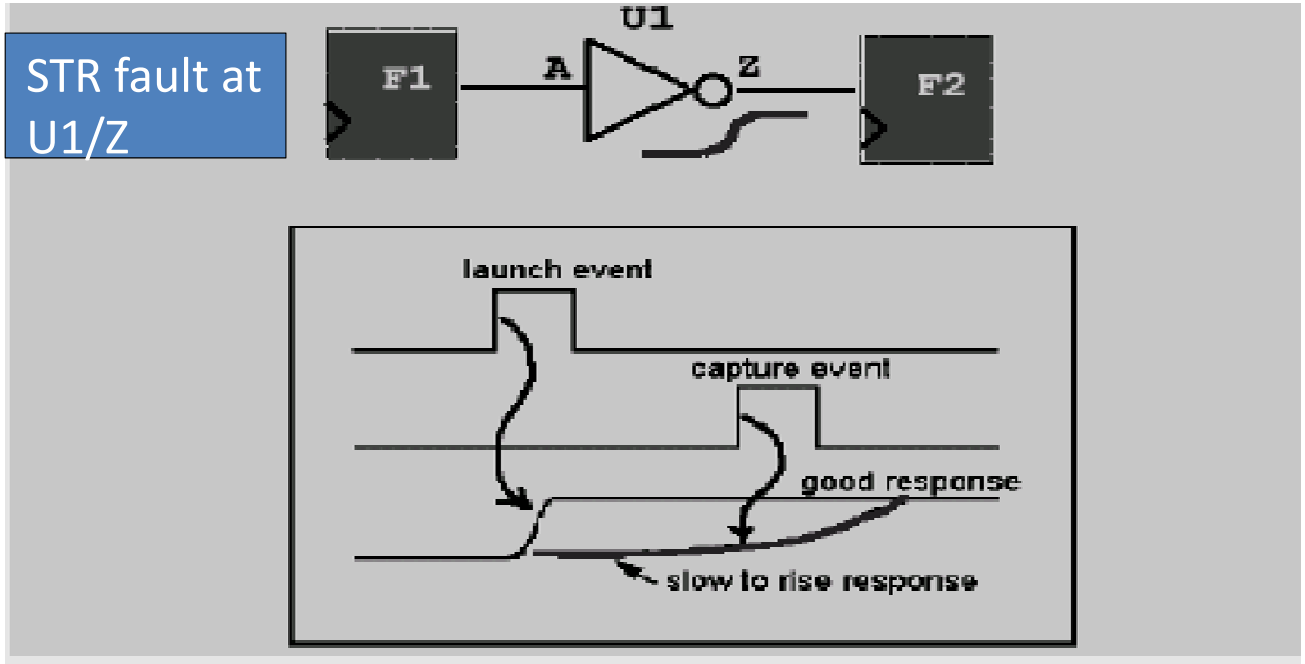
- Stuck-at fault model
- Delay fault model
  - Transition
  - path delay
- IDDQ

SA fault modeling



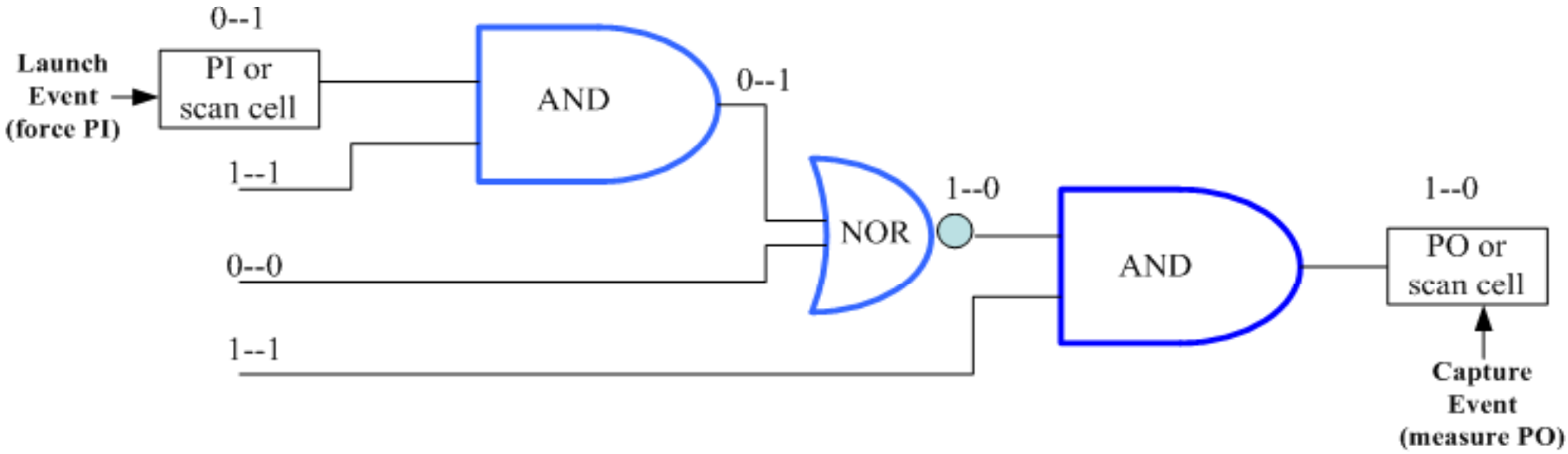
Transition fault modeling

- Focus on speed/timing
  - STR，(slow-to-rise)
  - STF，(slow-to-fall)



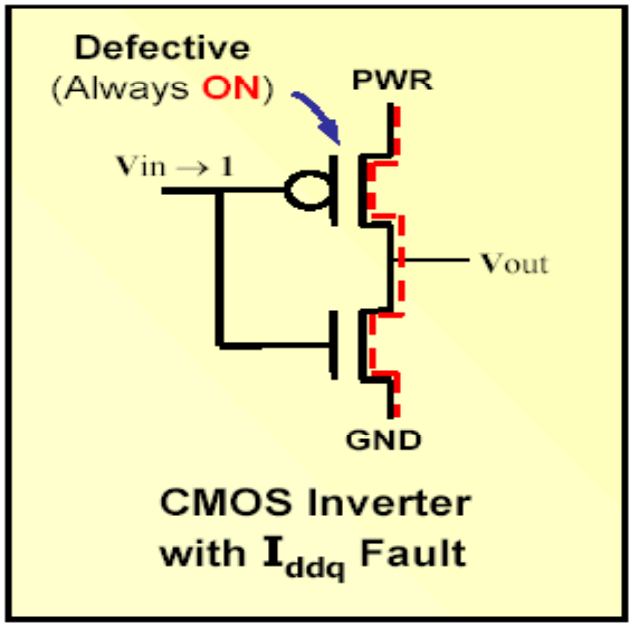
Path delay fault modeling

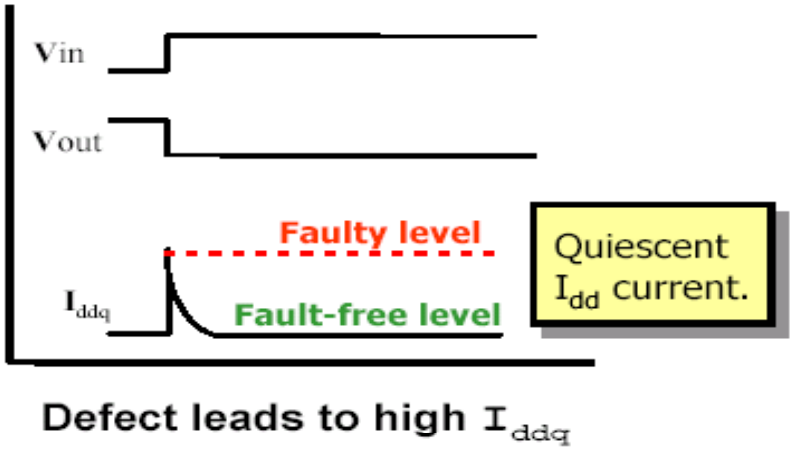
- Path delay faults do not have localized fault sites, rather, they are associated with testing the combined delay through all gates of specific paths.



IDDQ

- IDDQ: total current consumption when CMOS circuit in static state
- Just leakage current or diode reverse current,
- Any bridge, open, short or lead to IDDQ variation





Defect leads to high I_{ddq}

TetraMAX
IddQTest