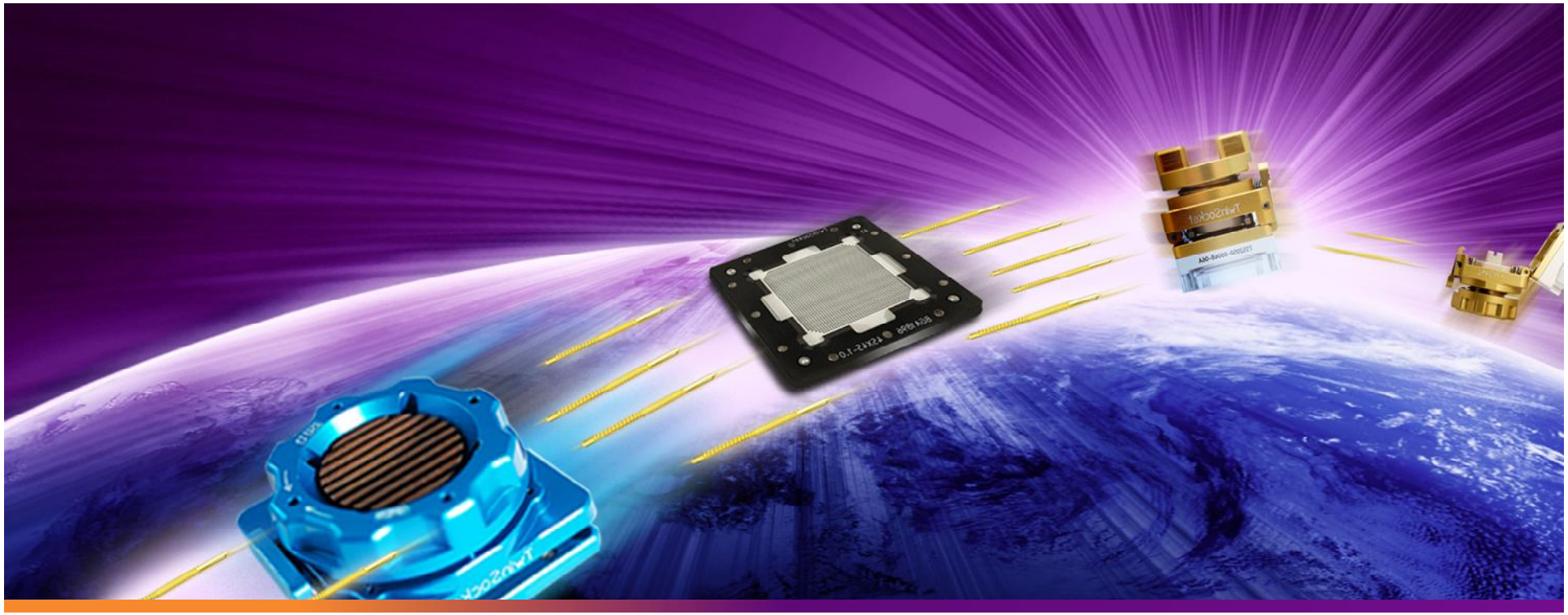
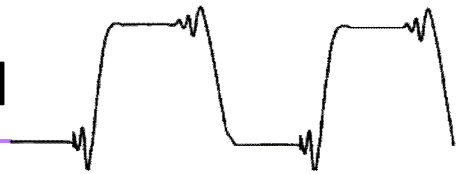
TwinSolution



Breaking the limit of high speed signal

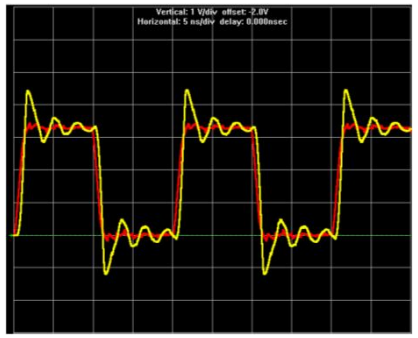


Twinsolution Engineering

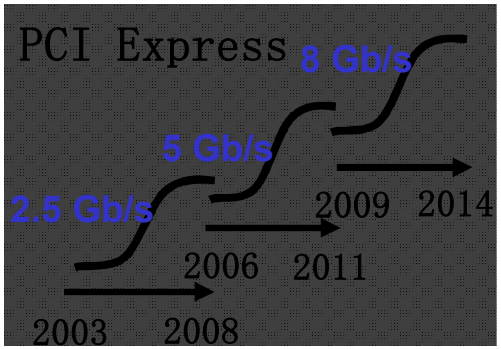
2015.07.14

Think big, start small

当今高速数字设计的挑战



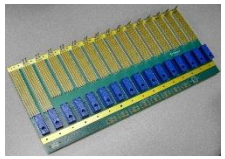
- **更高的信号速率引起显著的信号完整性(SI)和电源完整性(PI)的问题:**
  - 需要考虑板级，连接器，电缆等互连的高频效应
  - 需要更高质量的探头和测试夹具
  - 需要尽量降低抖动



- **标准规范以每2-3年的速度快速演进:**
  - 以现有的设计进展将更困难
  - 更紧的裕度对测量提出更大的挑战

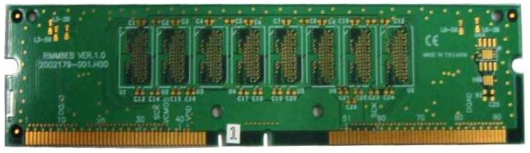
- **FPGAs更加广泛的应用:**
  - 简单的采用参考设计不再可行
  - 对于整体性能的模拟变得更困难
  - 需要对I/O 进行定性分析

高速互连面临挑战

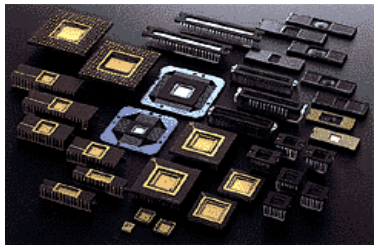


背板

连接器

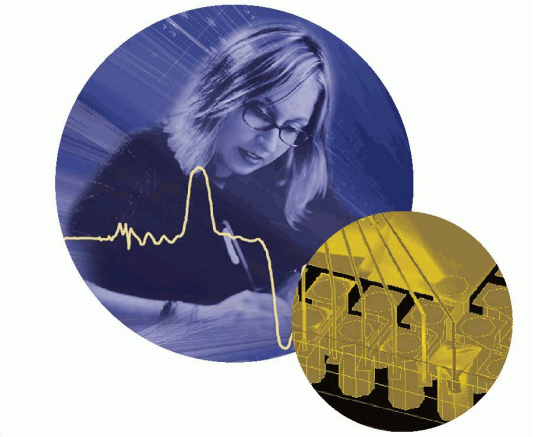


PCB

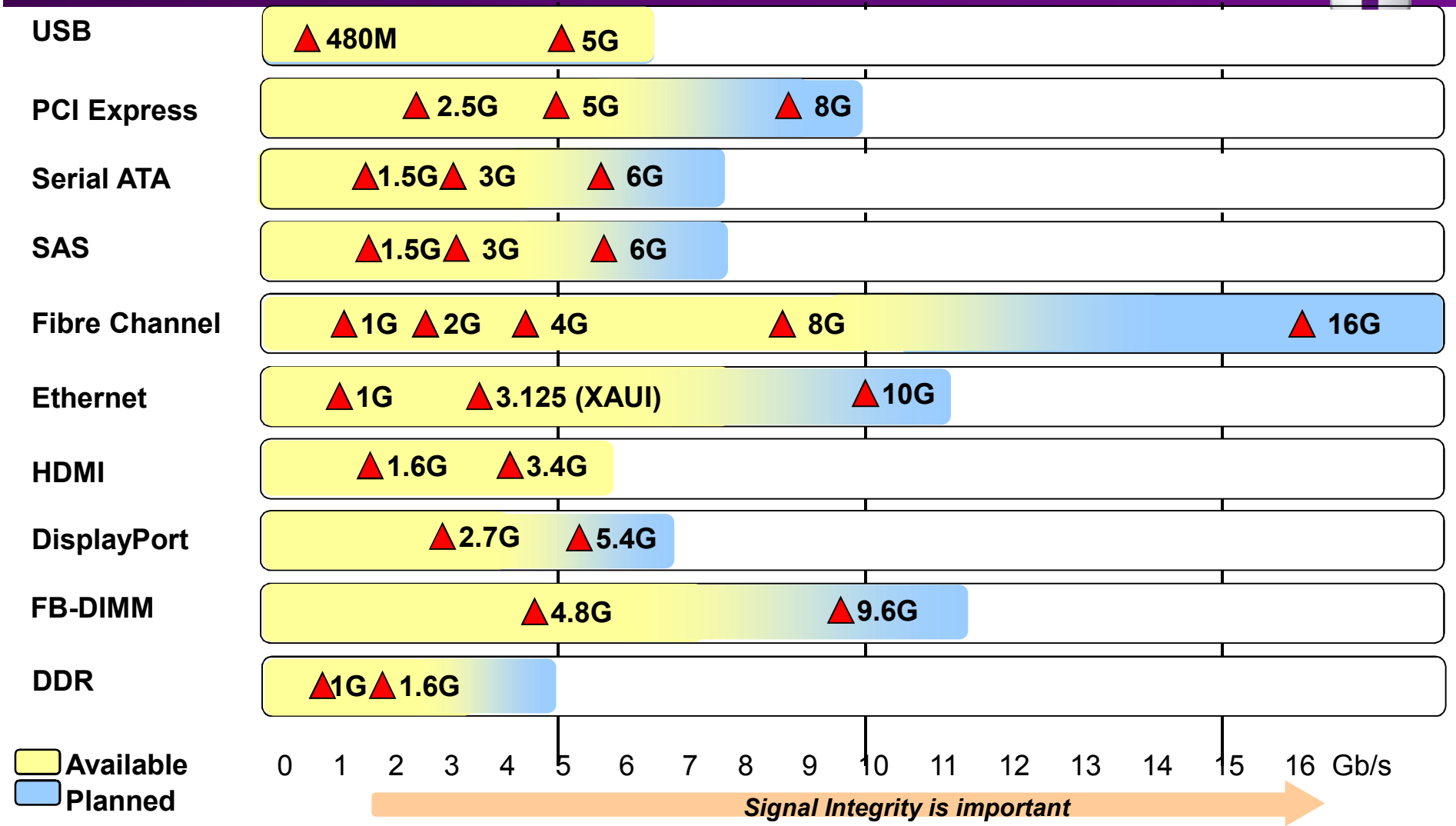


芯片封装

电缆

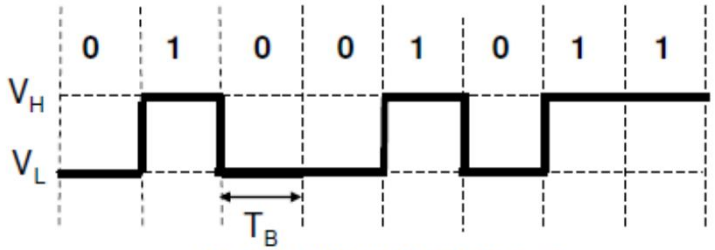


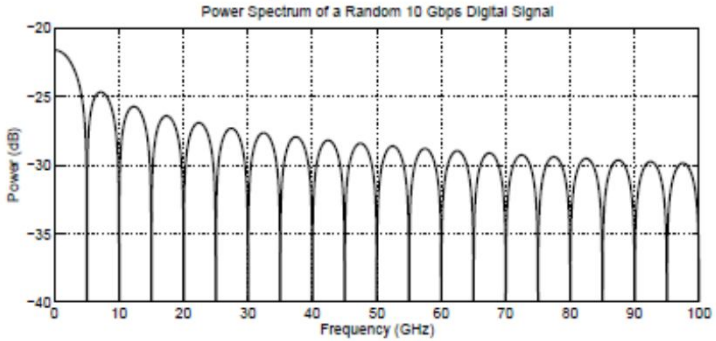
The Importance of Test Contactors for High-Speed Digital Device Testing

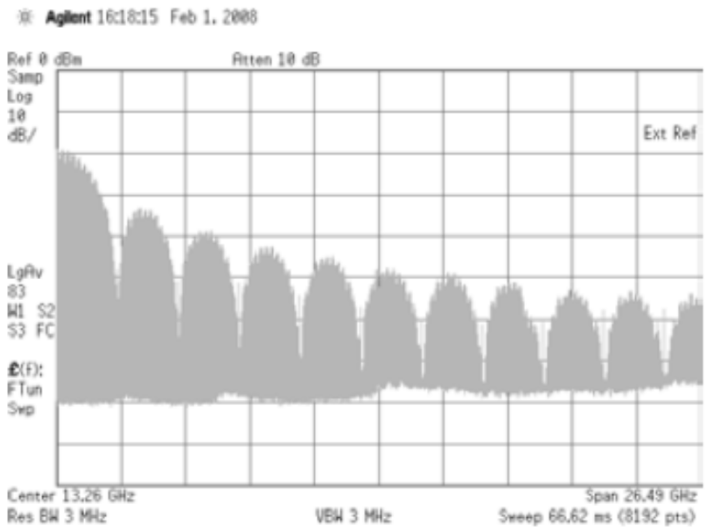


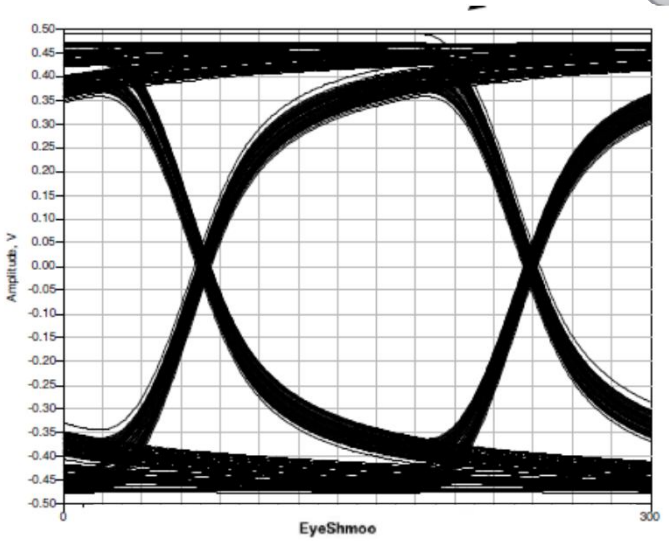
1. Memory interfaces are also increasing; LPDDR3 architectures are currently running at 800MHz, and the bandwidth is 12.8GBps. LPDDR4 is running at 1.6GHz, and the bandwidth is 24.8GBps.
2. SerDes Port : 30GHz

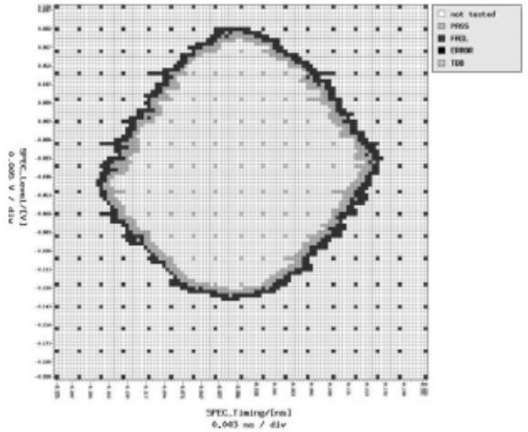
What Makes High-Sped Digital a Challenge?







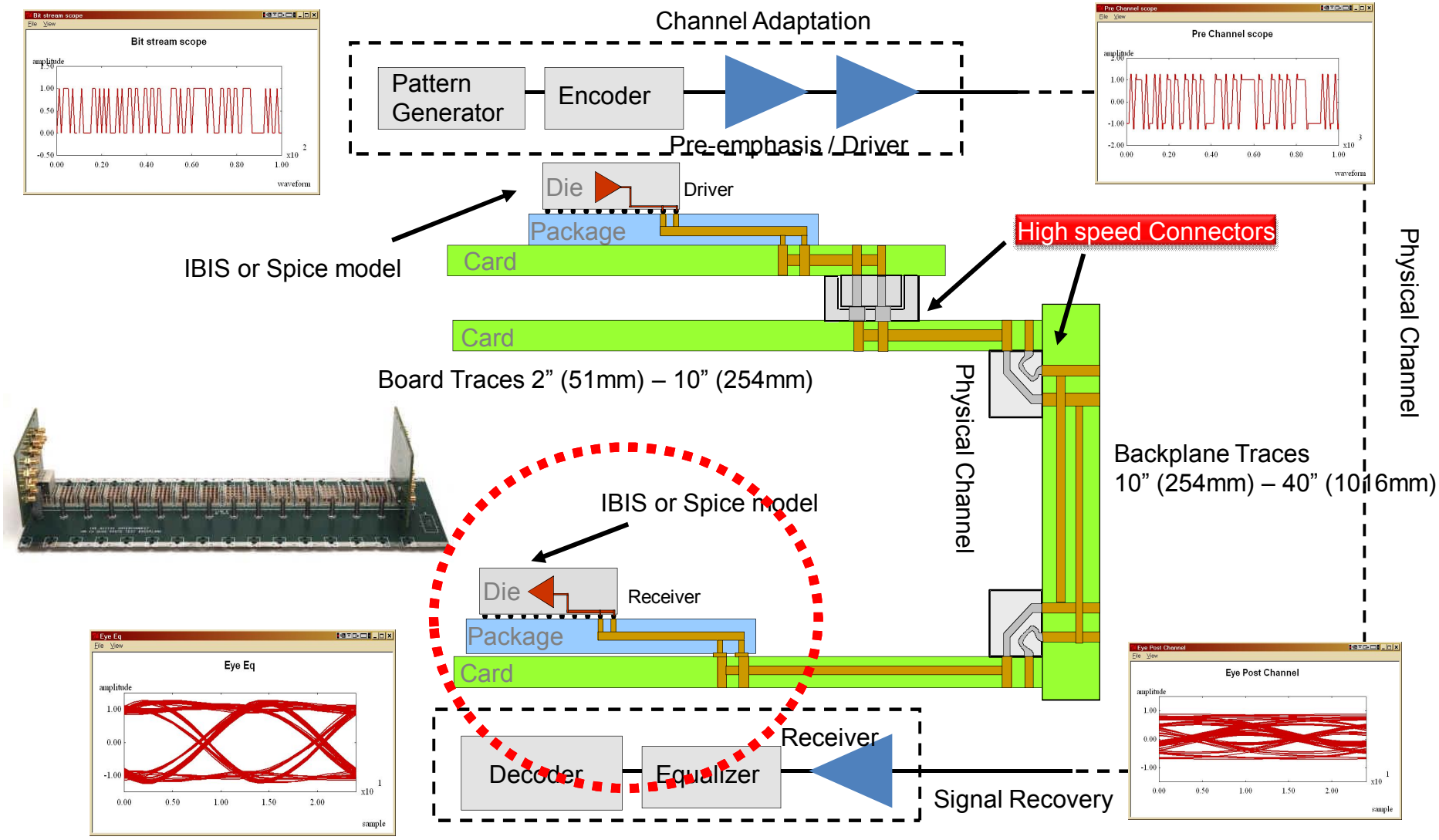




To convert this rise and fall time into its -3dB equivalent bandwidth use the well known formula **<u>BW= 0.34/rise time</u>**.

TwinSolution

高速系统的典型信号完整性问题



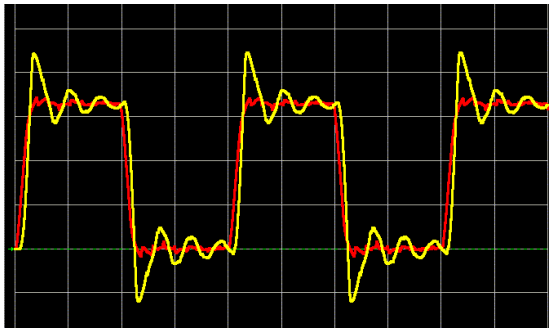
TwinSolution

Key Points

- Controlled Impedance
- Ultra Low Inductance

四种主要的信号完整性问题及成因

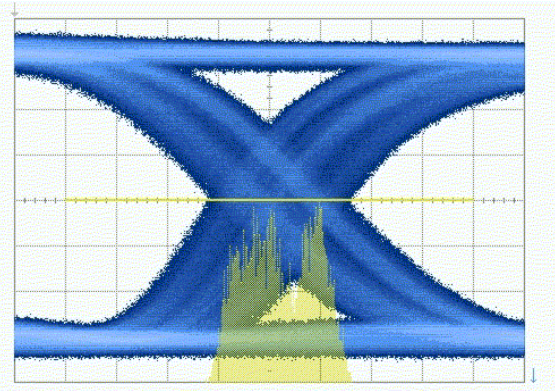
1. 单一网络的信号品质：
   在信号路径和回流路径上存在阻抗不连续导致信号的反射和失真问题



2. 在信号网络之间存在的串绕问题：
   互感和互容的存在

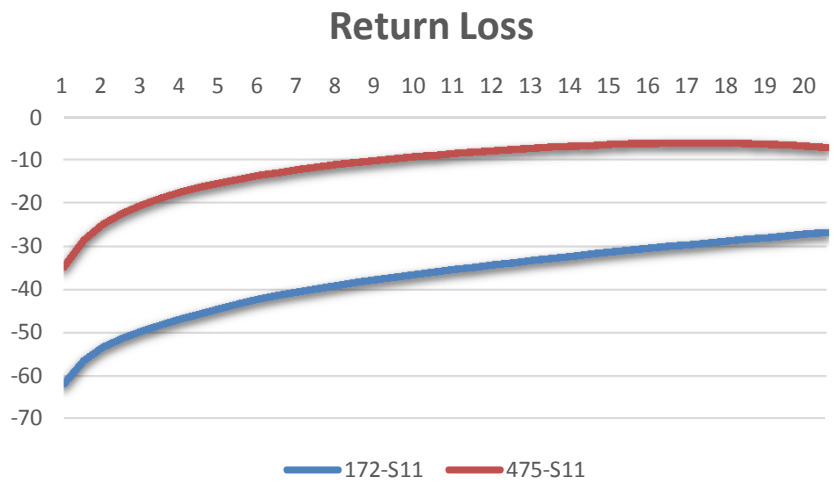
3. 在电源分布系统中的轨道塌陷噪声(地弹)：
   芯片等I/O开关切引起的暂态电流在电源/地网络平面导致电压跌落

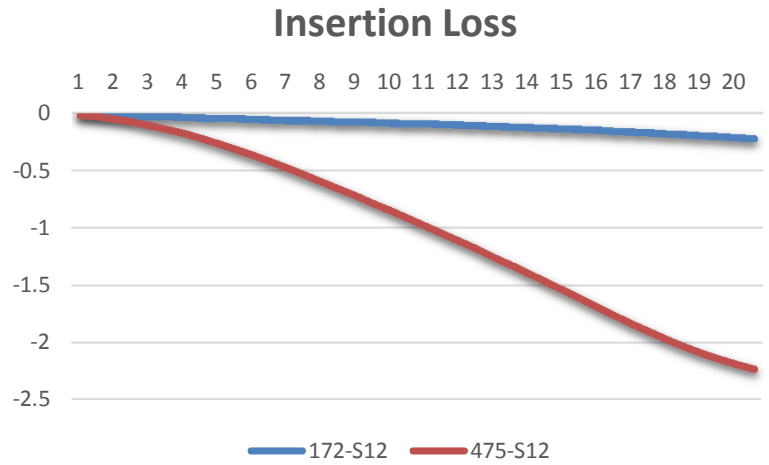
4. 抖动的问题：
   以上的问题可能引起抖动；
   时钟分布，数据相关的因素，以及EMI也可能引起抖动的问题



信号的质量

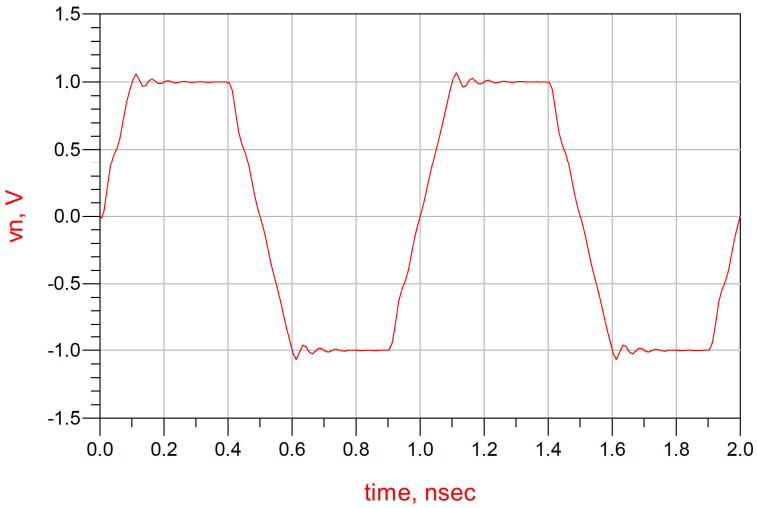
SI- Single Signal Integrity



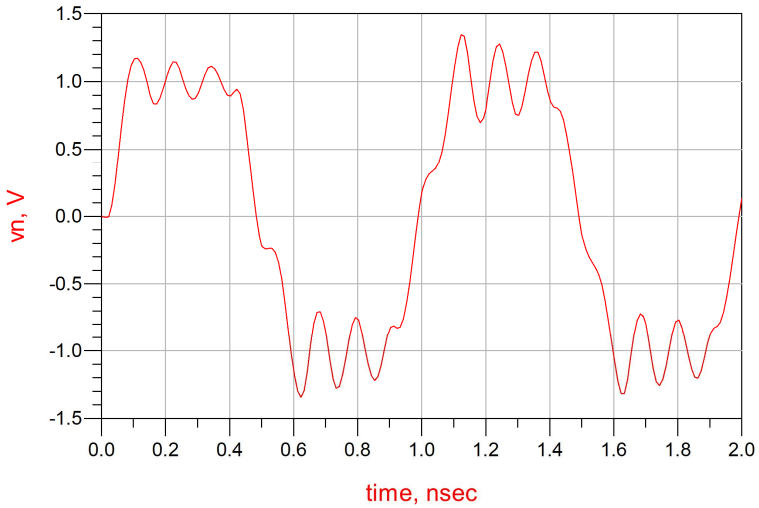


SI- Single Signal Integrity

172 Pin



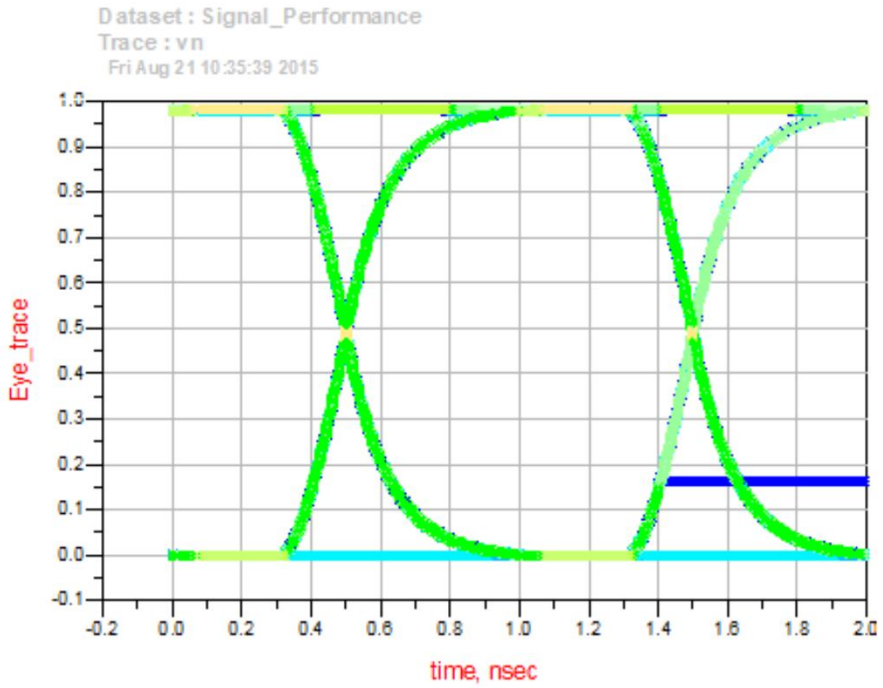
475 Pin



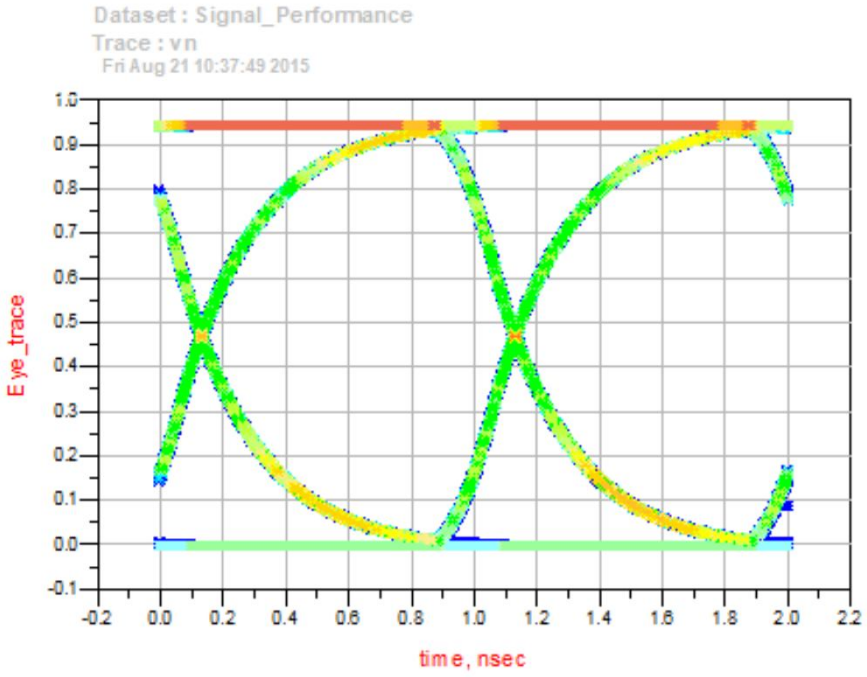
1GHz 的方波信号输入

SI- Single Signal Integrity

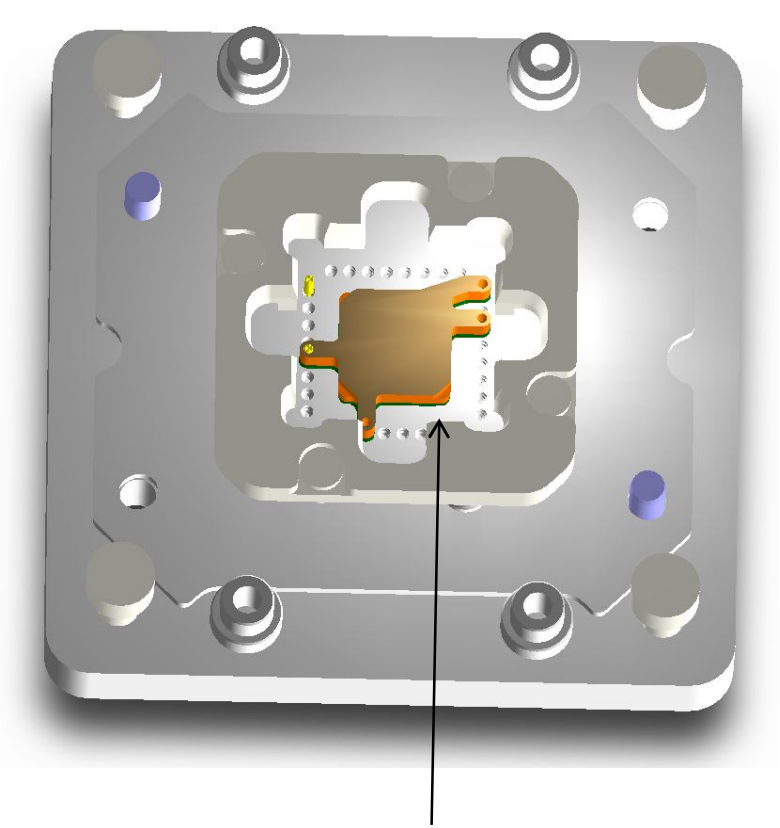
172 Pin



475 Pin



Octopus – Grounding Redistribution



Center Grounding Redistribution Copper Block

- Pitch 800um
- Pin Length: 2.85mm
- Device: 6GHz
- Status:
  - ✓ Customer Mass Production

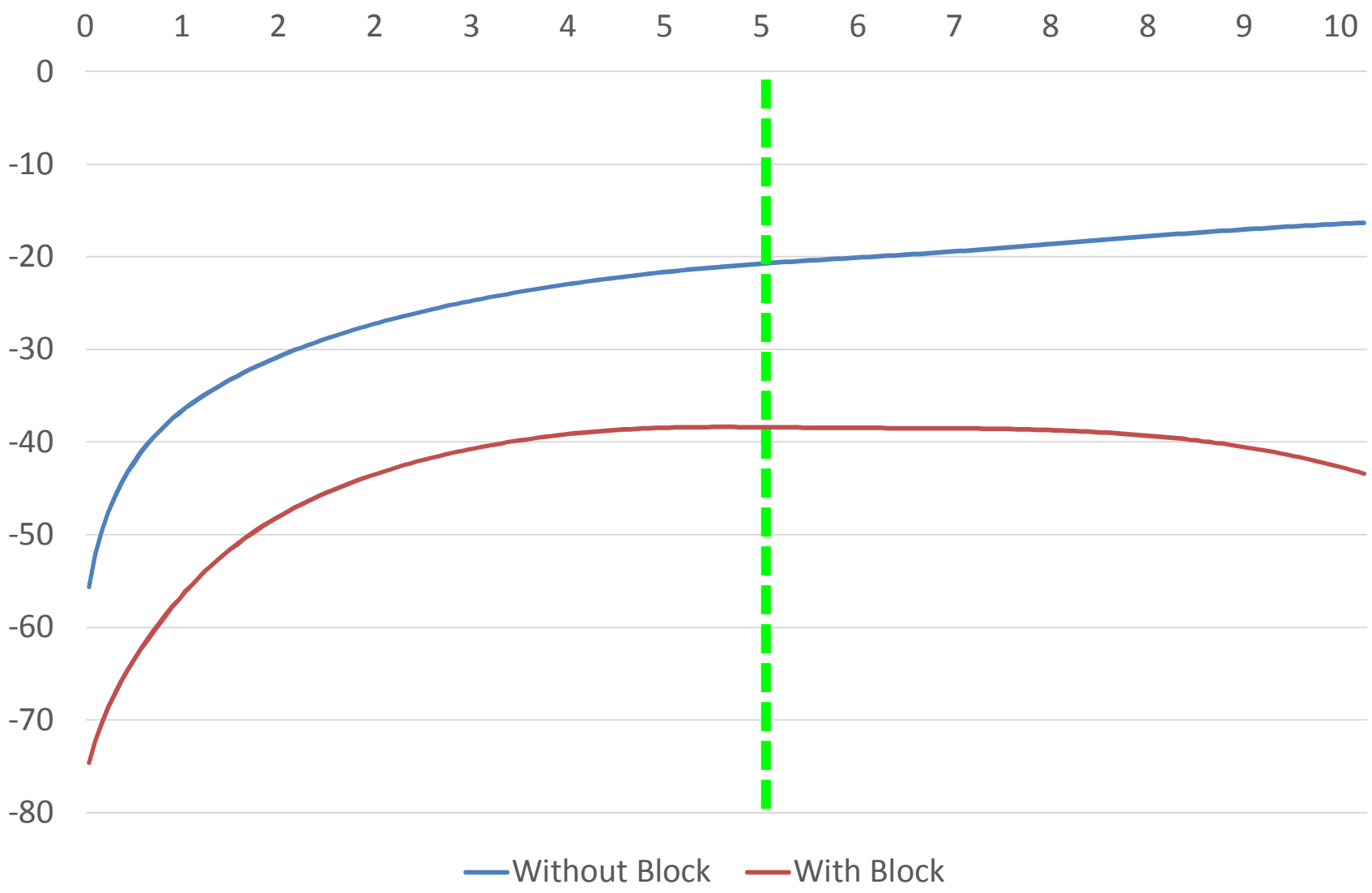
- RF Performance:

  - Insertion Loss< -0.1dB @ 2.4GHz

  - Return Loss < -25dB @ 2.4GHz

  - Power Loss: -0.8dBm (Improved around 1.5dBm)

SI- Single Signal Integrity

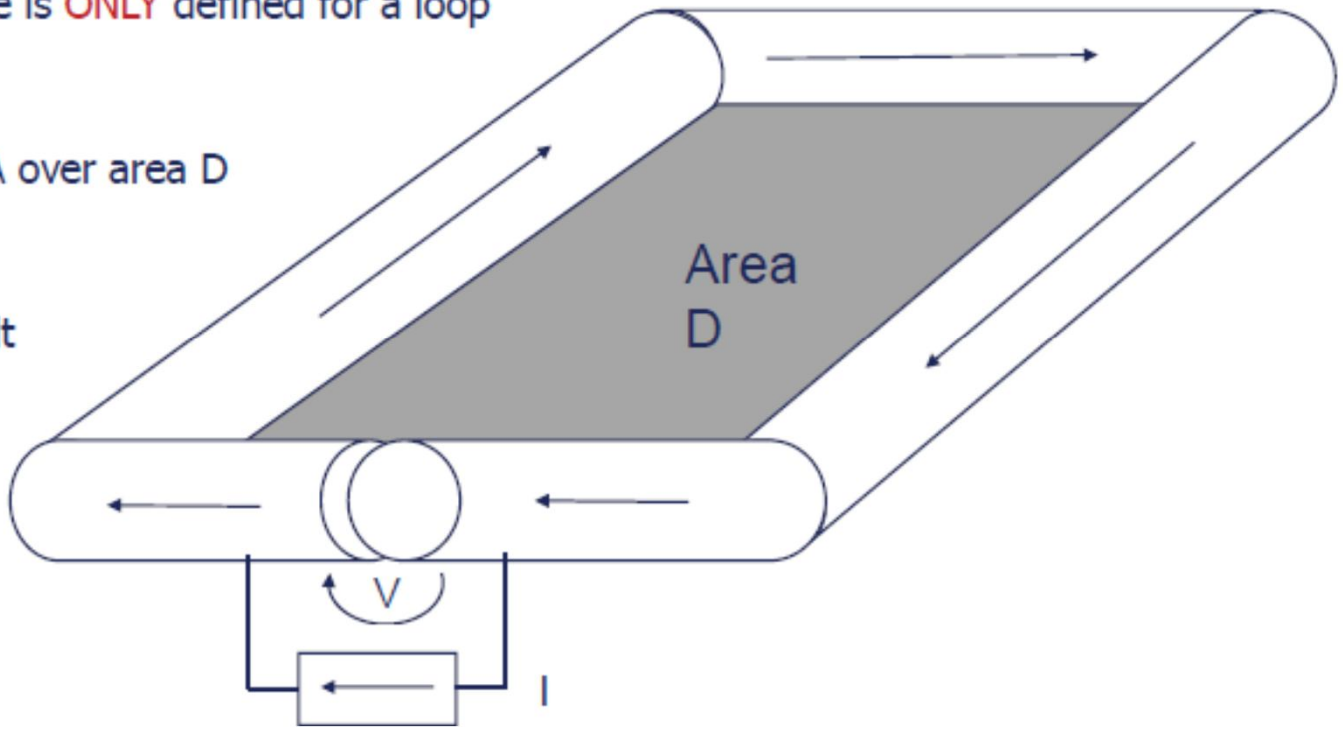


SI- Cross Talk

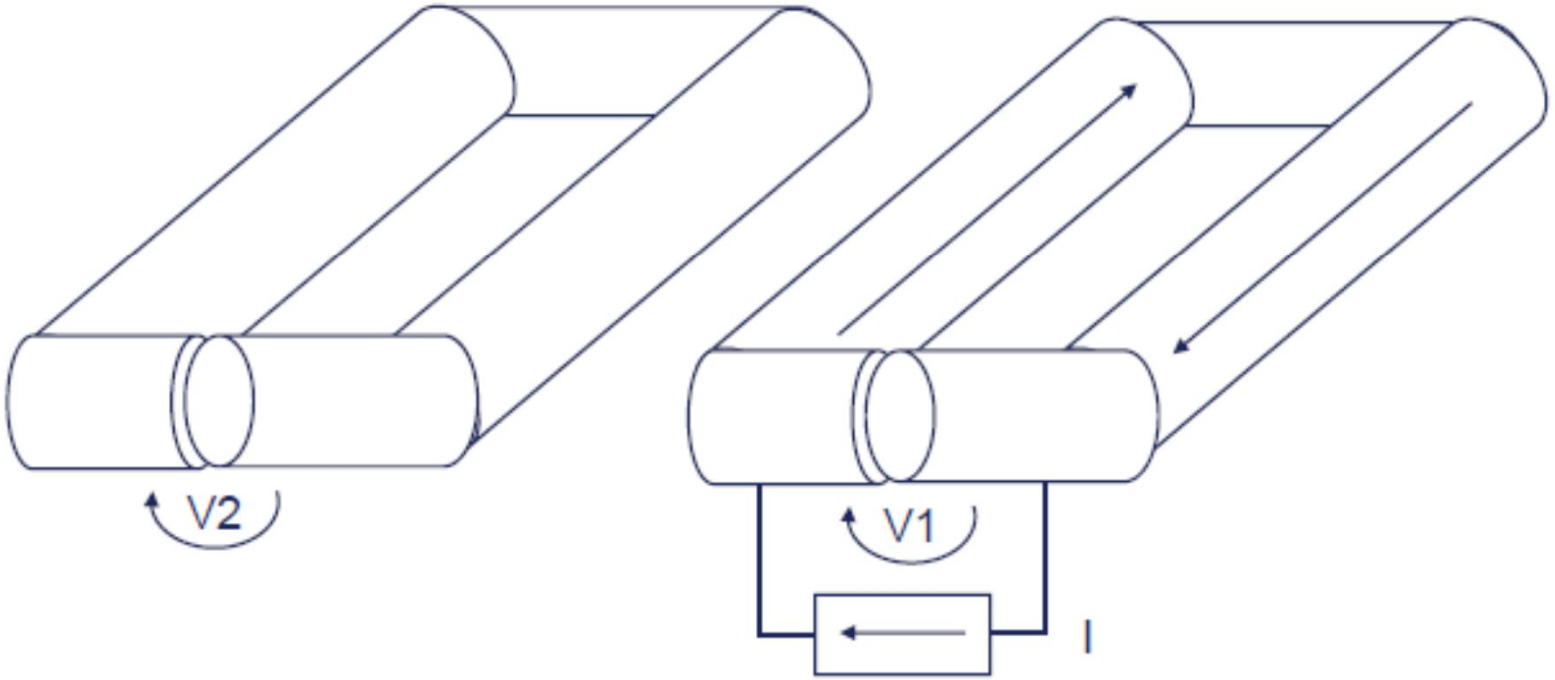
- Mutual Inductance
- Mutual Capacitance

Definition of Inductance

- Inductance L is magnetic flux through a loop area divided by the current
- Inductance is ONLY defined for a loop
- $\Phi = \int B \cdot dA$ over area D
- $L = \Phi / I$
- $V = L \, dI/dt$



Self and Mutual Inductance



- Self loop inductance generates a voltage V1 in the driven loop
- Mutual loop inductance generates a voltage V2 in the adjacent loop
  - Note – current in adjacent loop is 0

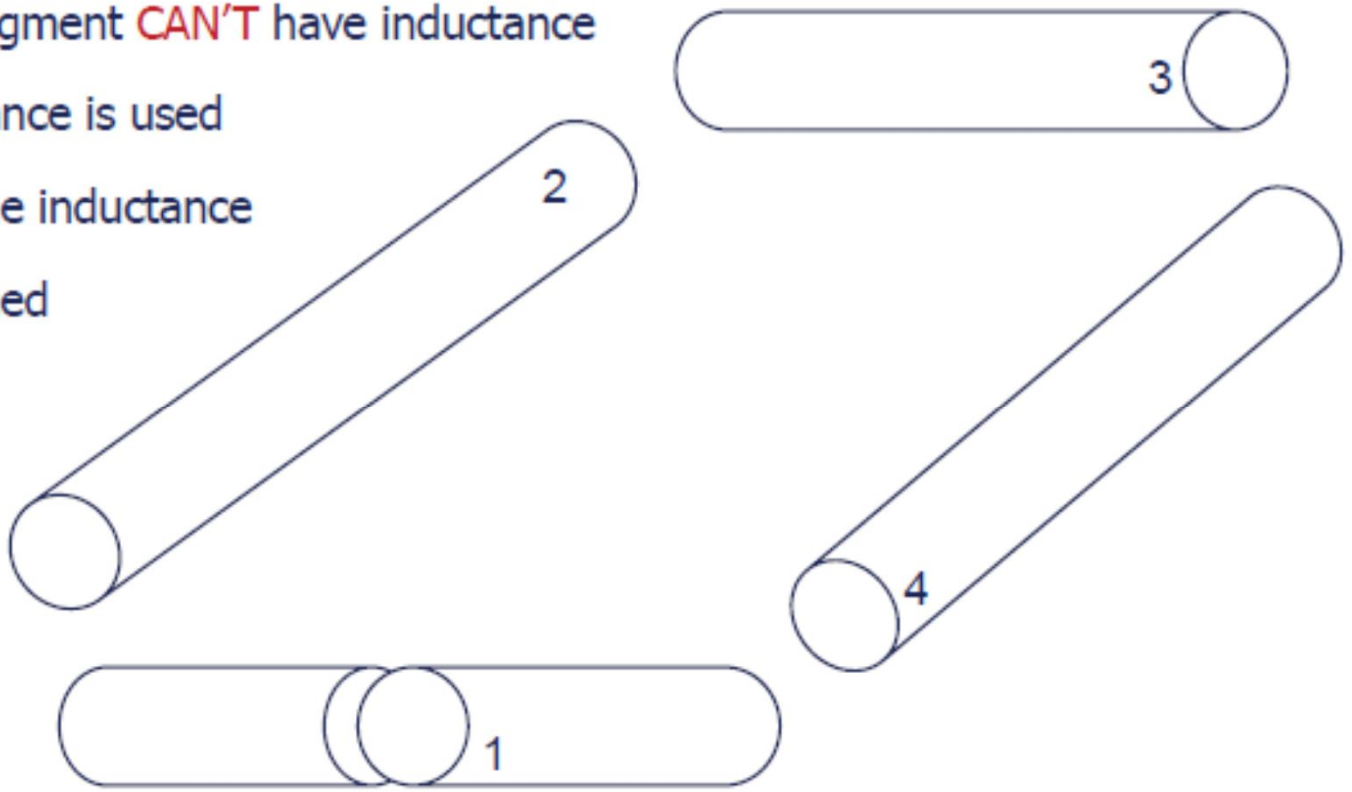
Partial Inductance

- Partial Inductances are the Self and Mutual Inductances of the loop segments
- Mathematical construct - They have NO MEANING independent of other partial inductances that form a loop
- An isolated segment CAN'T have inductance
- Partial inductance is used

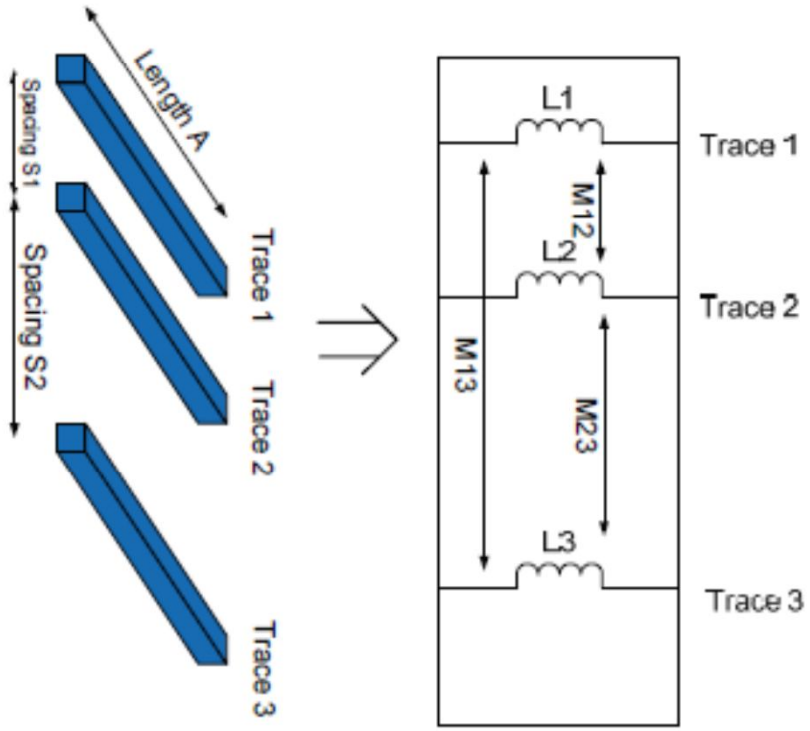
  to calculate the inductance

  of a loop formed

  of segments



3D Field Solver Partial Inductances



- 3 Traces in Free Space (no reference plane in structure)
  - Typical for 2 layer packages
- L1, L2, L3 – **Partial** Self Inductances are determined mostly by length, smaller effects from width and height
- M12, M23, M13 – **Partial** Mutual Inductances mainly a function of spacing and length

3D Field Solver Inductance Matrix

	Trace 1	Trace 2	Trace 3
Trace 1	5.16	3.78	0.458
Trace 2	3.78	5.16	0.464
Trace 3	0.458	0.464	5.16

Partial Mutual Inductance

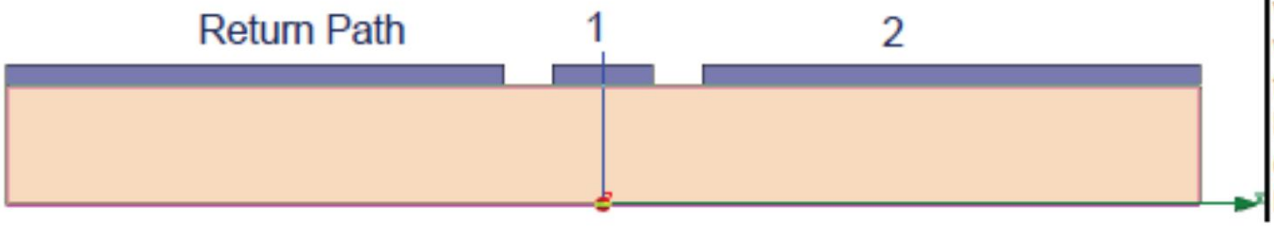
Partial Self Inductance

- ONLY LOOP INDUCTANCE HAS MEANING
- To define loops, the current paths must be defined
- Example: Trace2 is a return path
  - Trace1 to Trace2 loop = 5.16+5.16-2*3.78 = 2.76
  - Trace3 to Trace2 loop = 5.16+5.16-2*0.464 = 9.39

Why Partial Inductances are Misleading

- Actual test case comparing various extraction tools
- Question? Which tool gives the correct partial inductances? Is conductor 1's self partial inductance 4.5 or 10.1?
- Answer? They are all correct! Partial inductance is only meaningful with respect to other partial and mutual inductances within a loop. Partial inductances can't be compared between tools or even different simulations on the same tool. Only loop inductances can be compared. In this case they are all within about 15%.

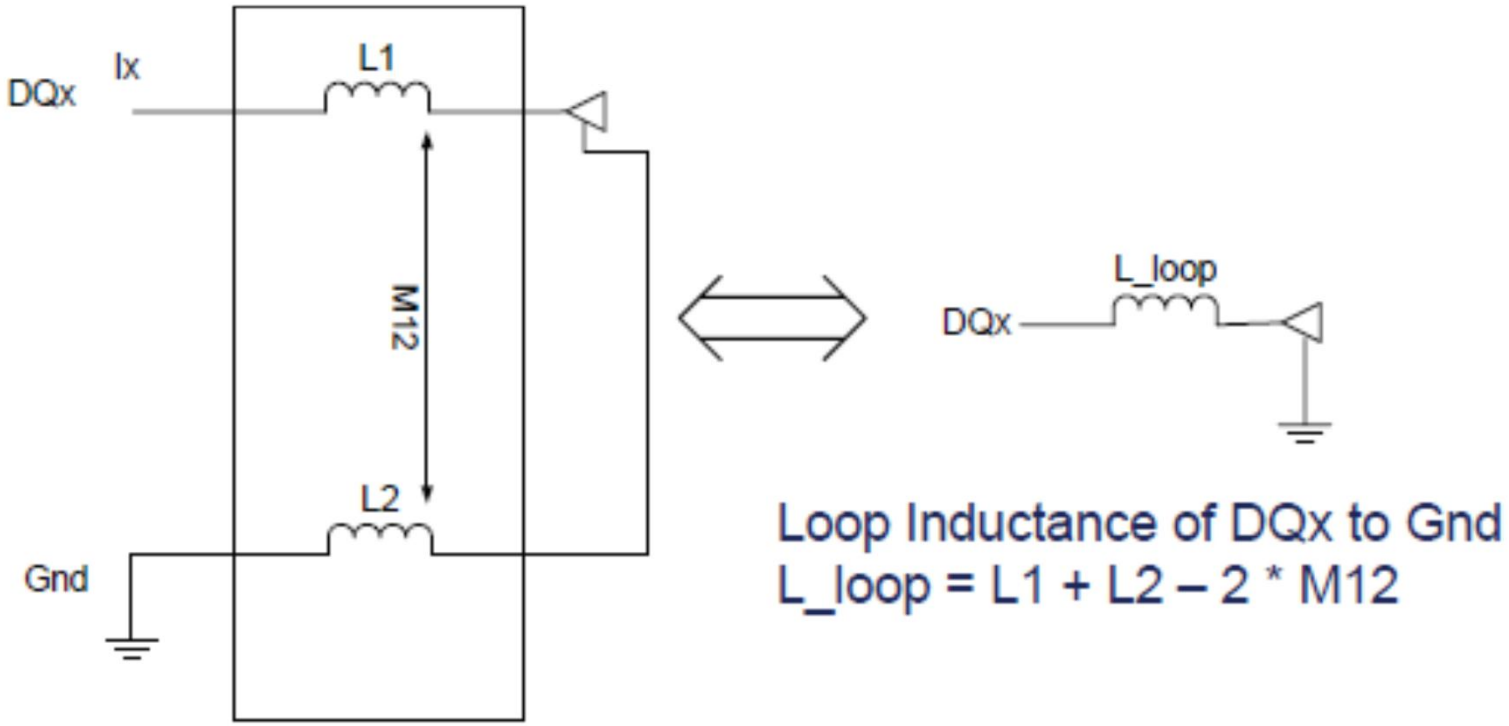
	A	B	C	D
Self Partial 1	5.280	4.533	10.072	10.100
Self Partial 2	5.856	5.375	9.022	9.261
Mutual 1-2	2.929	2.681	7.244	6.900
Loop 1-2	5.278	4.546	4.606	5.561



width of center trace	50 µm
width of reference	250 µm
width of gap	25 µm
thickness of trace/ref.	10 µm
height of substrate	60 µm
dielectric constant	4.5
length of trace	10 mm

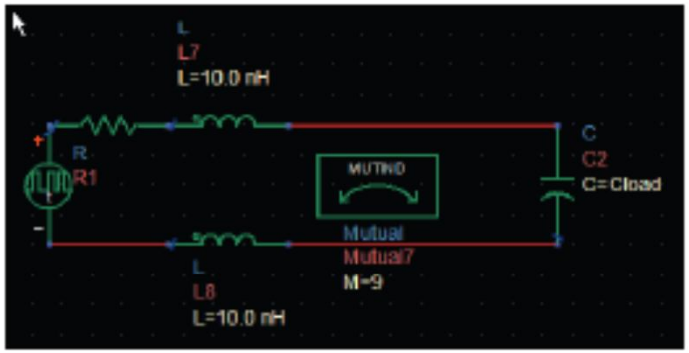
Signal Loop Inductance Model

These 2 circuits are equivalent



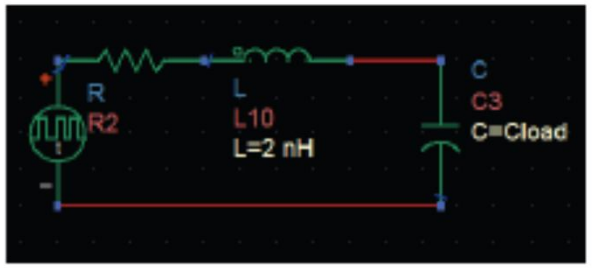
Loop Inductance of DQx to Gnd
L_loop = L1 + L2 – 2 * M12

Simulation with 2 Inductors

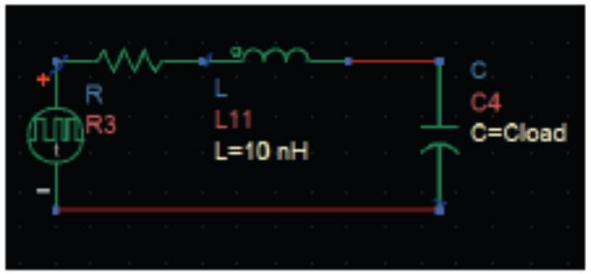


L-loop= 10 + 10 – 2*9 = 2 nH

Equivalent Circuits

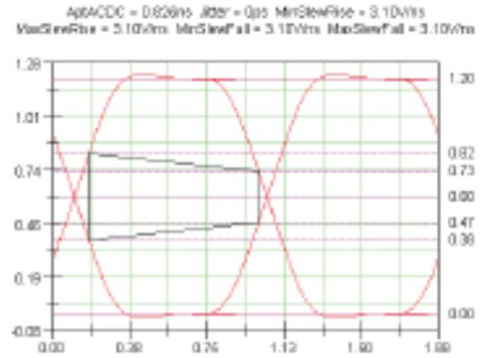


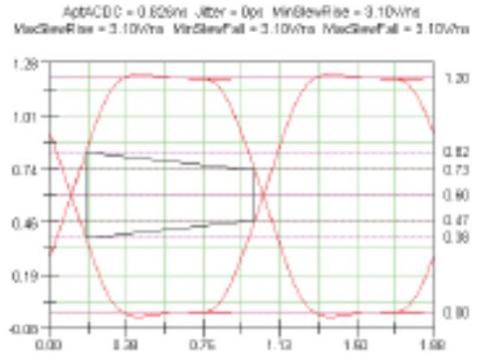
Single L=L_loop = 2nH

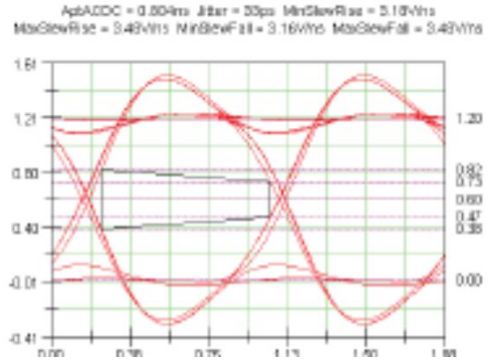


Single L=L_Partial = 10nH

Incorrect result using only partial inductance and ignoring mutual terms





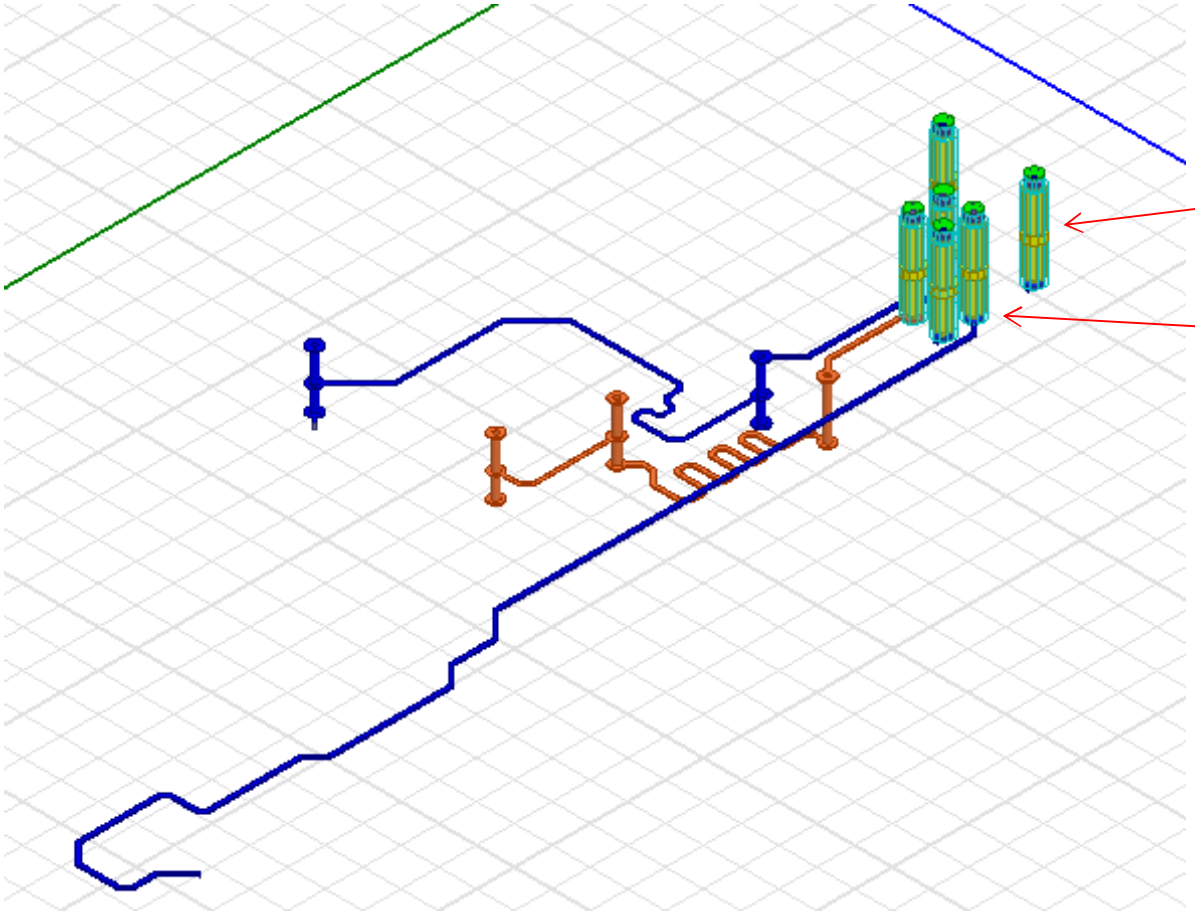


TwinSolution

SI- Cross Talk

Simulation Setup

BGA-Product

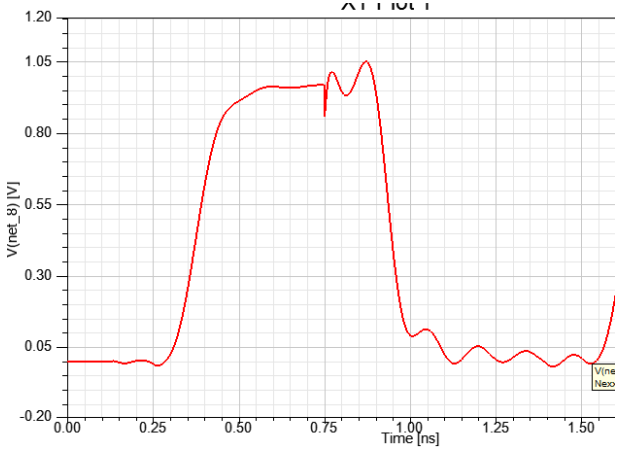


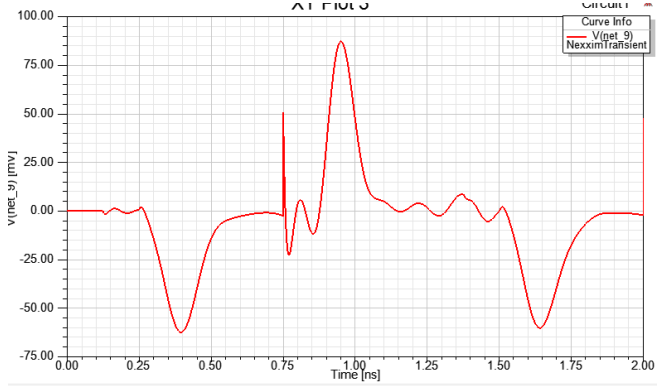
Socket Model

PCB Trace

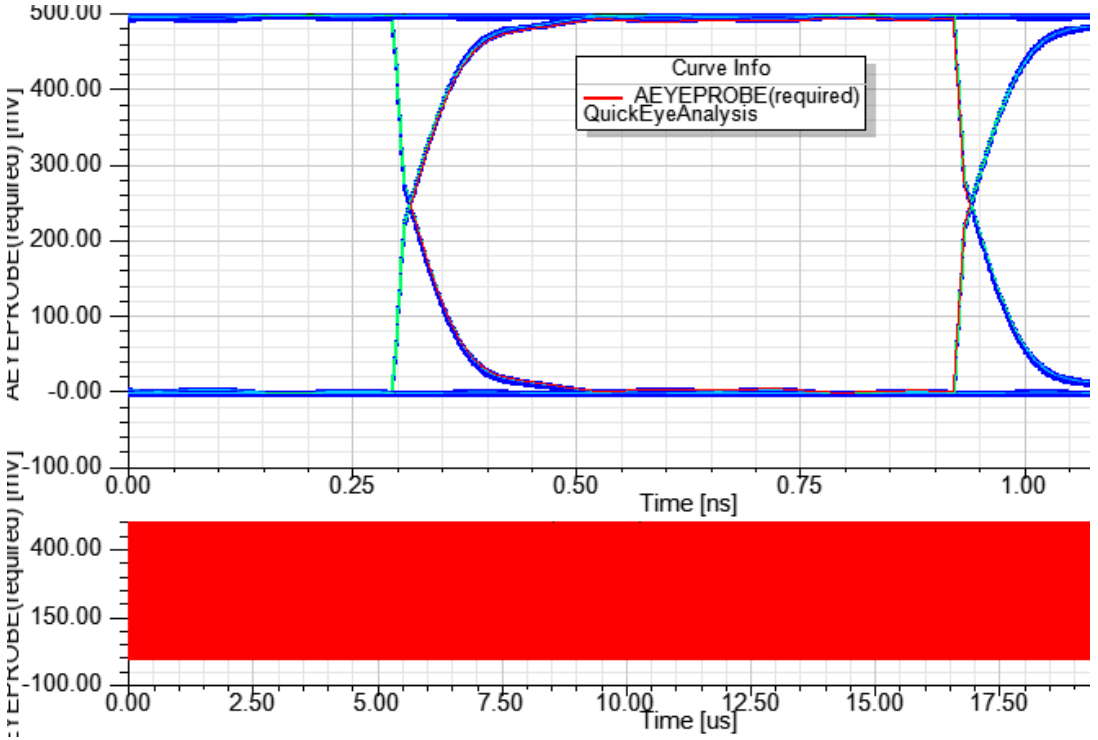
SI- Cross Talk

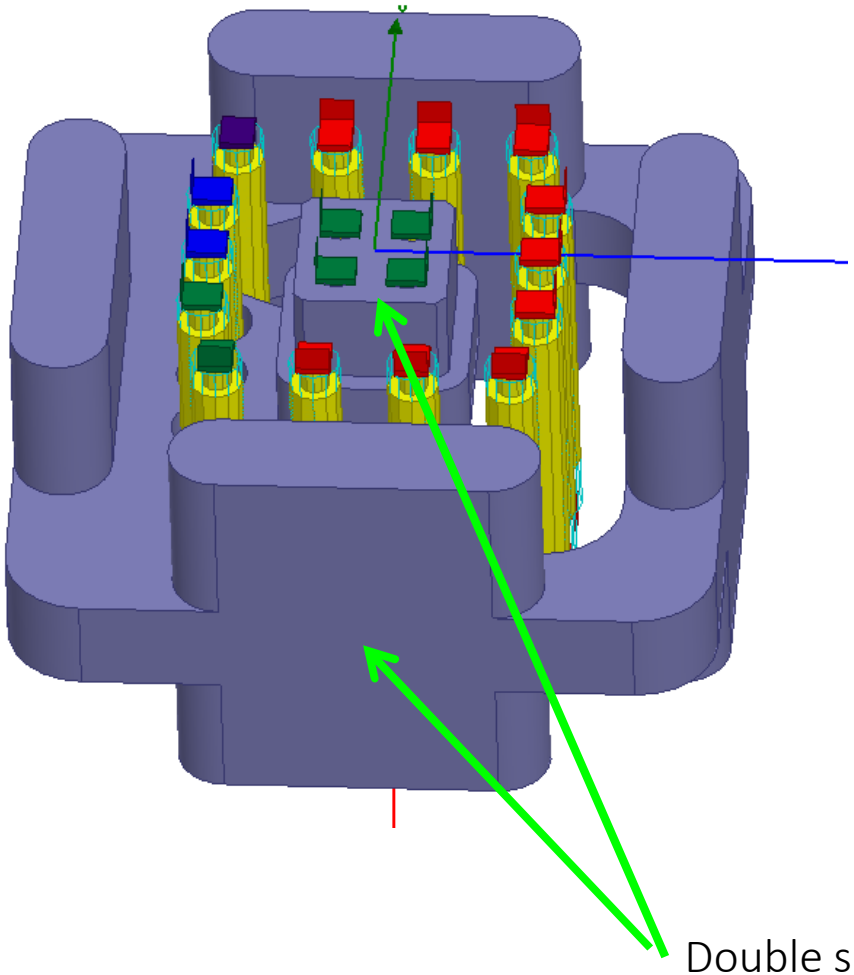
Result





Eye Diagram





Original Design:

- 0.2mm Pin Design
- Block Clearance: 0.3mm

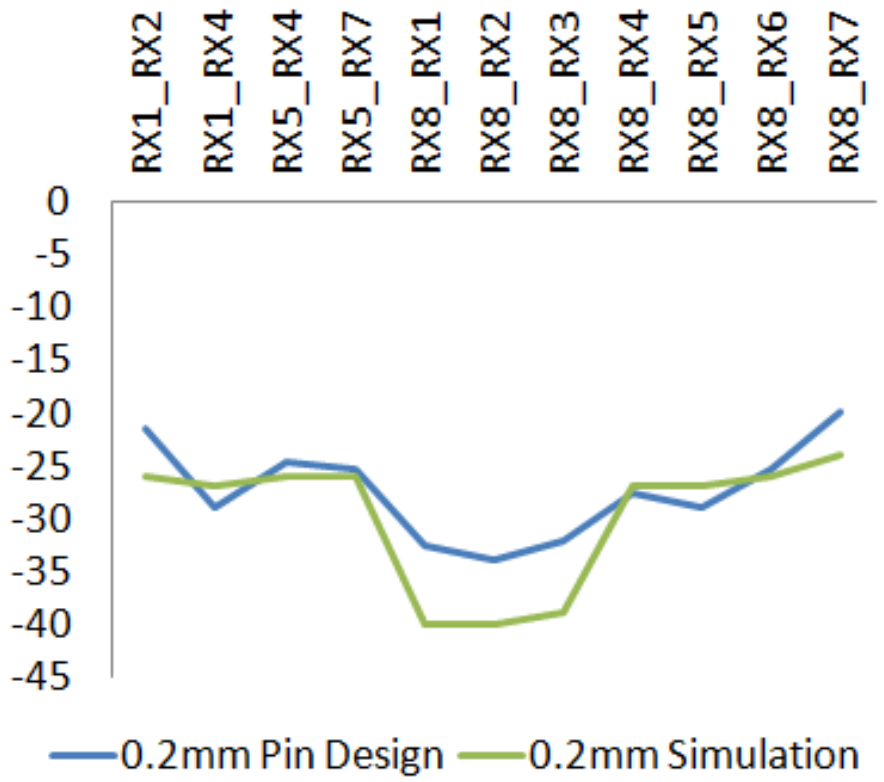
New Design:

- 0.26mm Pin Design
- Block Clearance: 0.36mm

Double side GND wrap.

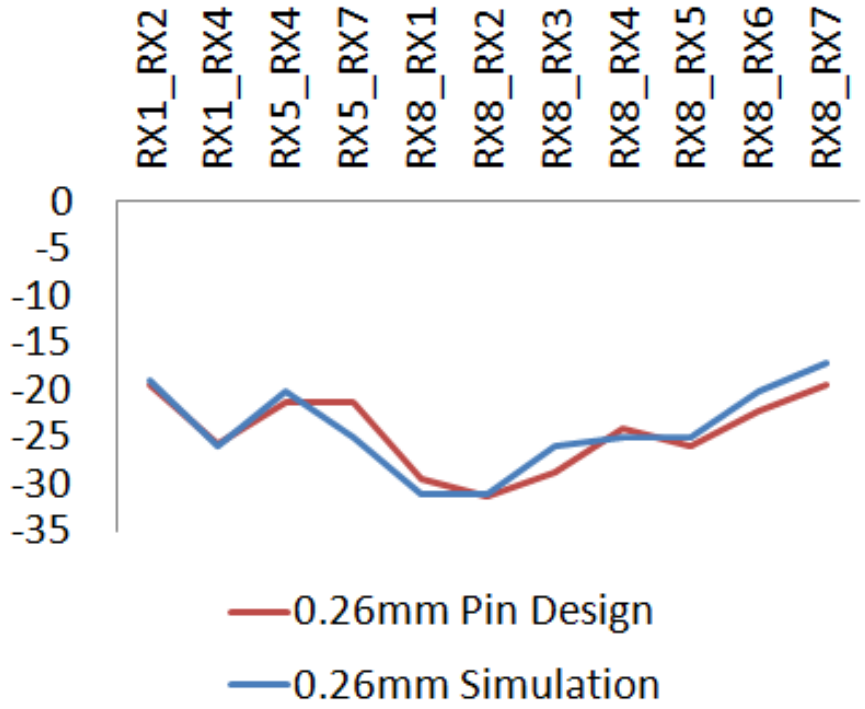
Isolation Data (Measurement Vs Simulation)

0.2mm Pin Design



Difference Average: 2.4dB

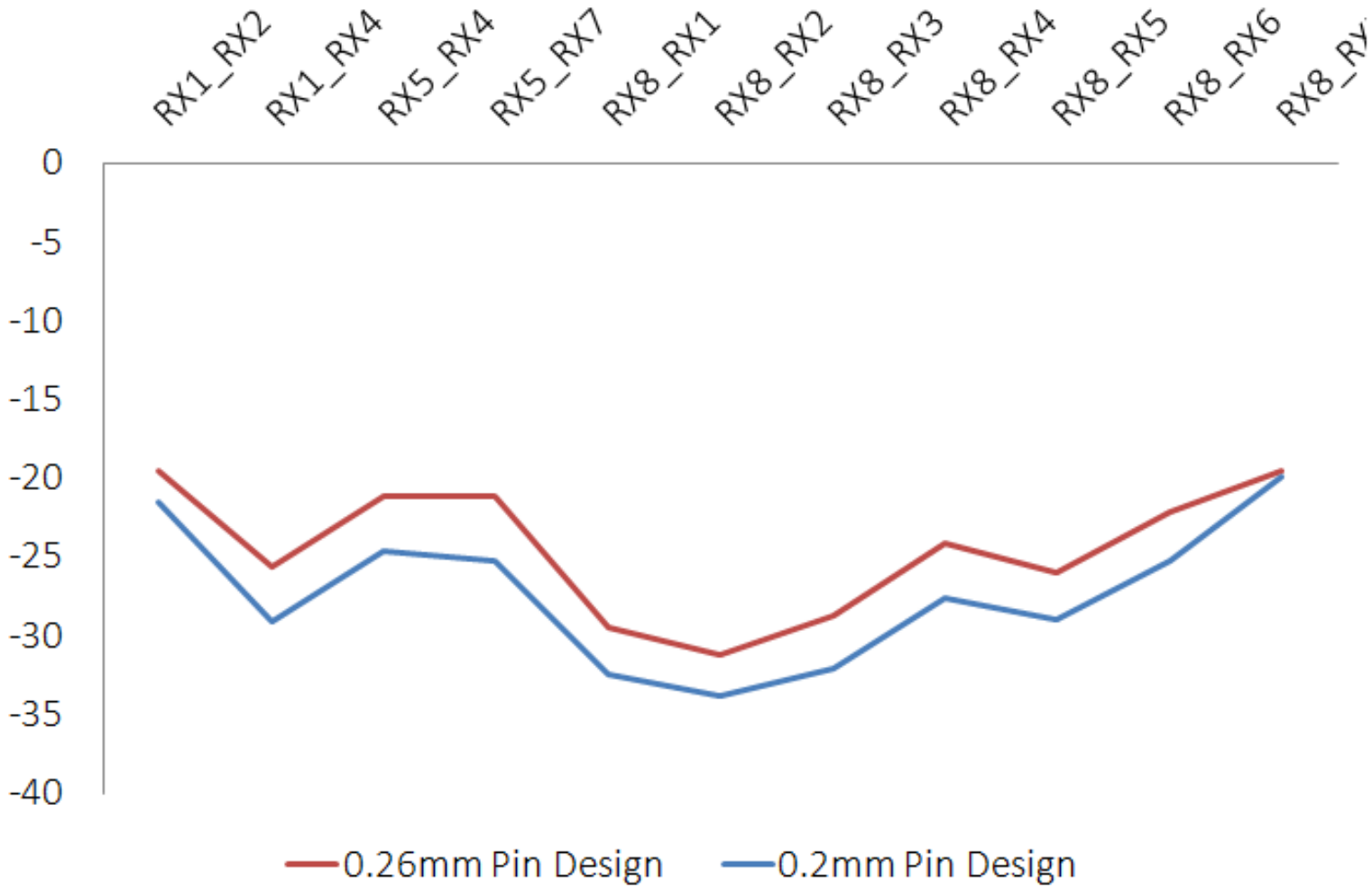
0.26mm Pin Design



Difference Average: 0.33dB

1. 0.2mm Pin design has a larger difference compare with 0.26mm pin design, might because of insufficient GND of the outside block.

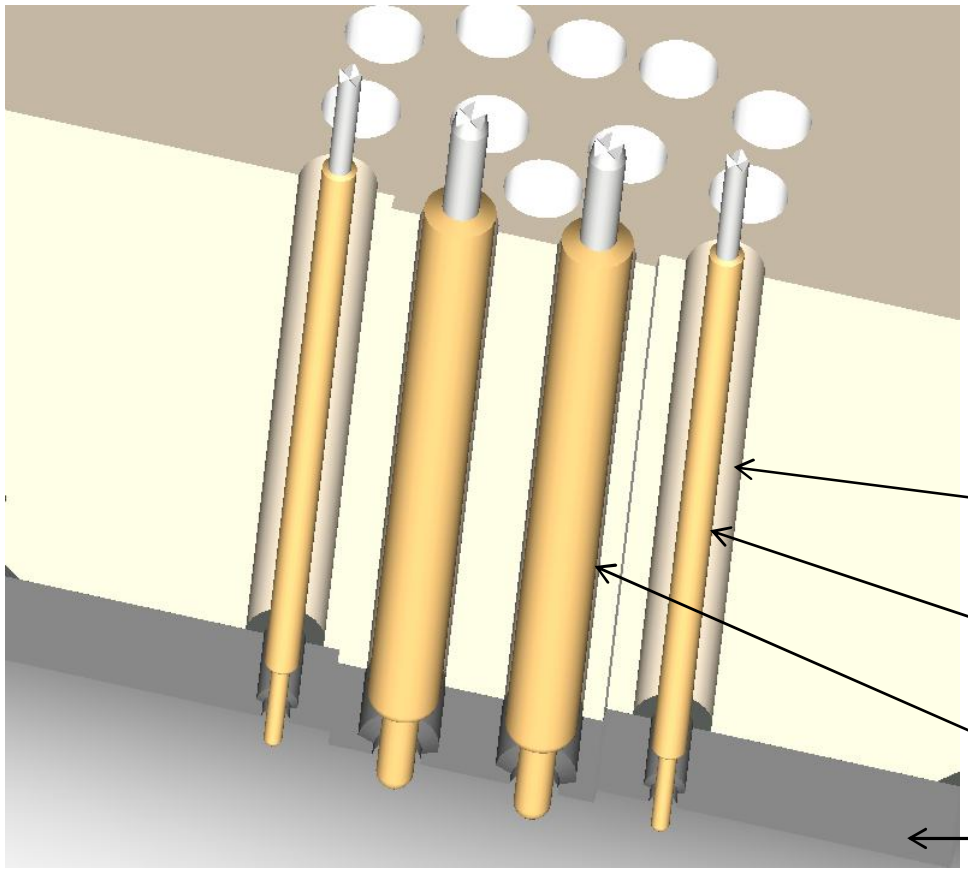
2 Design Isolation Comparison



1. 0.2mm Pin design has better absolute value compare with 0.26mm pin design.

Skyeye- Fine Pitch

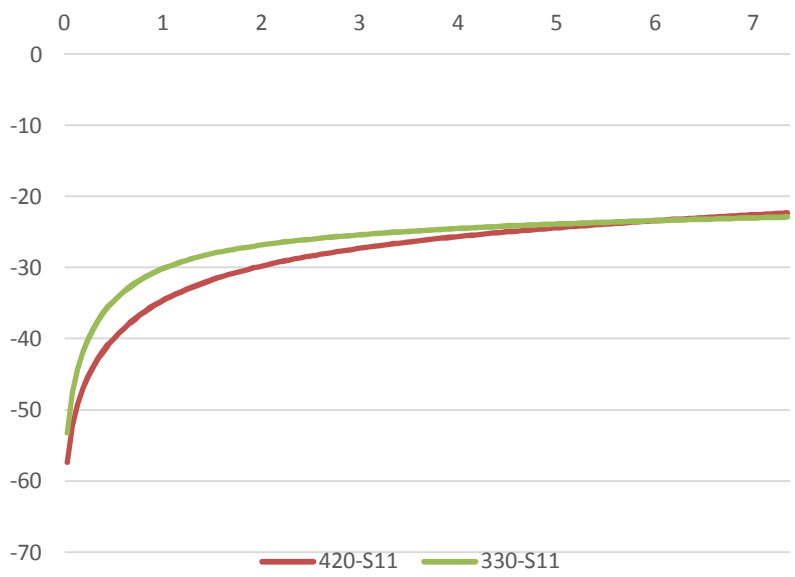
Socket Center Using Copper Block Grounding

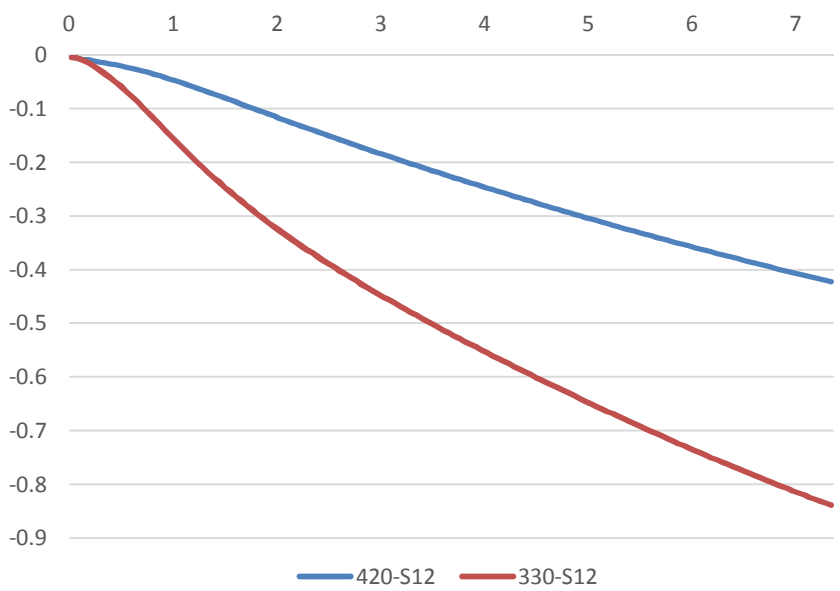


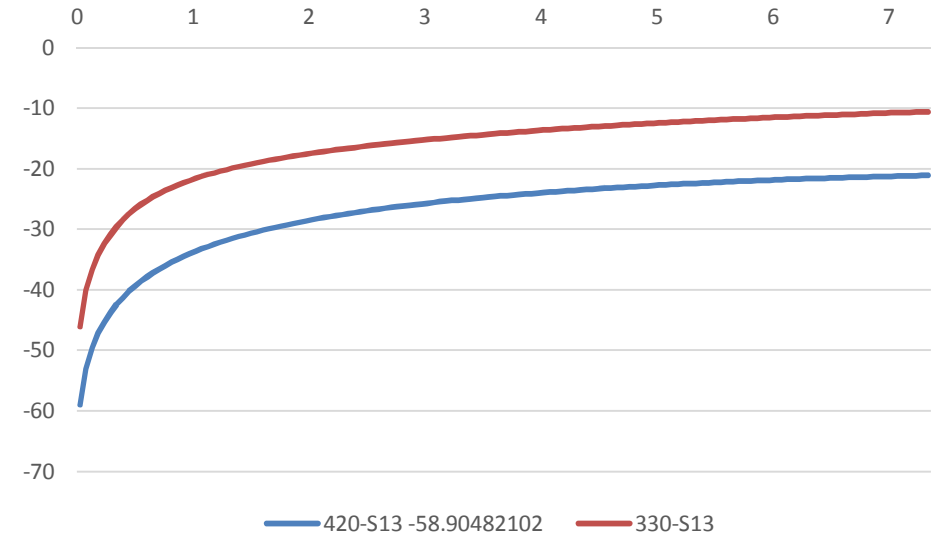
- Pitch Range : 300um to 500um
- Pin Length: 4.2mm
- Device: 20Gbps

- RF Performance:
  - Insertion Loss< -0.3dB @ 2.4GHz
  - Return Loss < -30dB @ 2.4GHz
  - Isolation< -21dB to -25dB @ 2.4GHz

Comparison With Traditional Socket







Isolation @ 2.4GHz
420: -20dB
330: -16dB

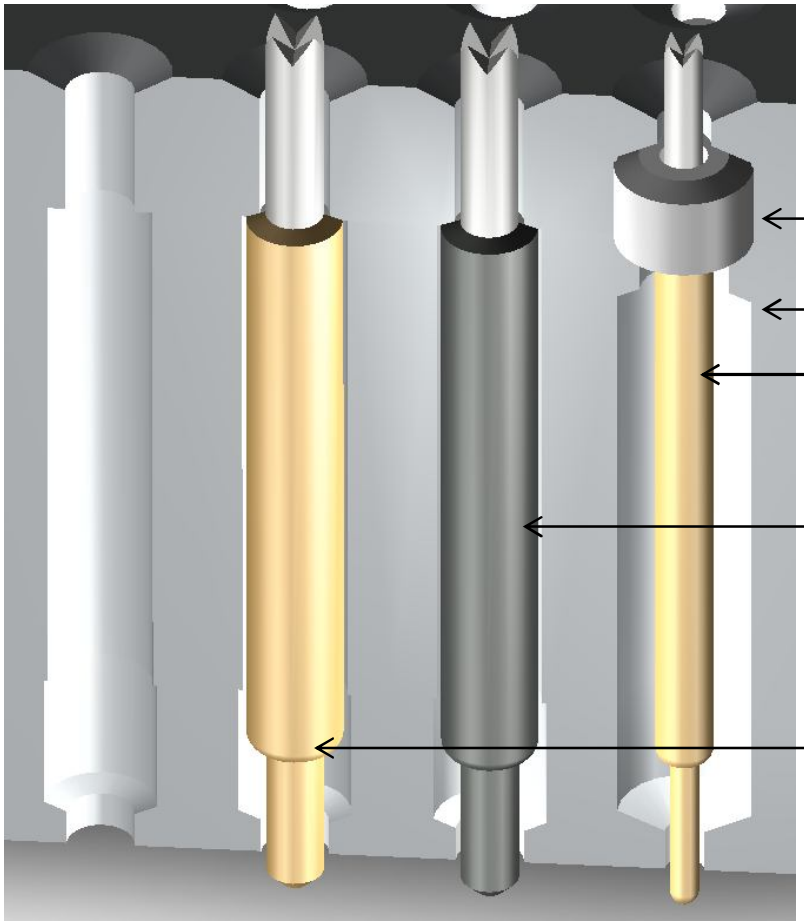
TwinSolution

Tesla- High Speed Digital

Full 50ohm Impedance Control
Coaxial Socket

- Pitch Range : 0.4mm to 1.27mm
- Device: 60Gbps / 40GHz

- DLC Coated Probe



Teflon Ring- Provide Insulation

Insulation Conductive Material

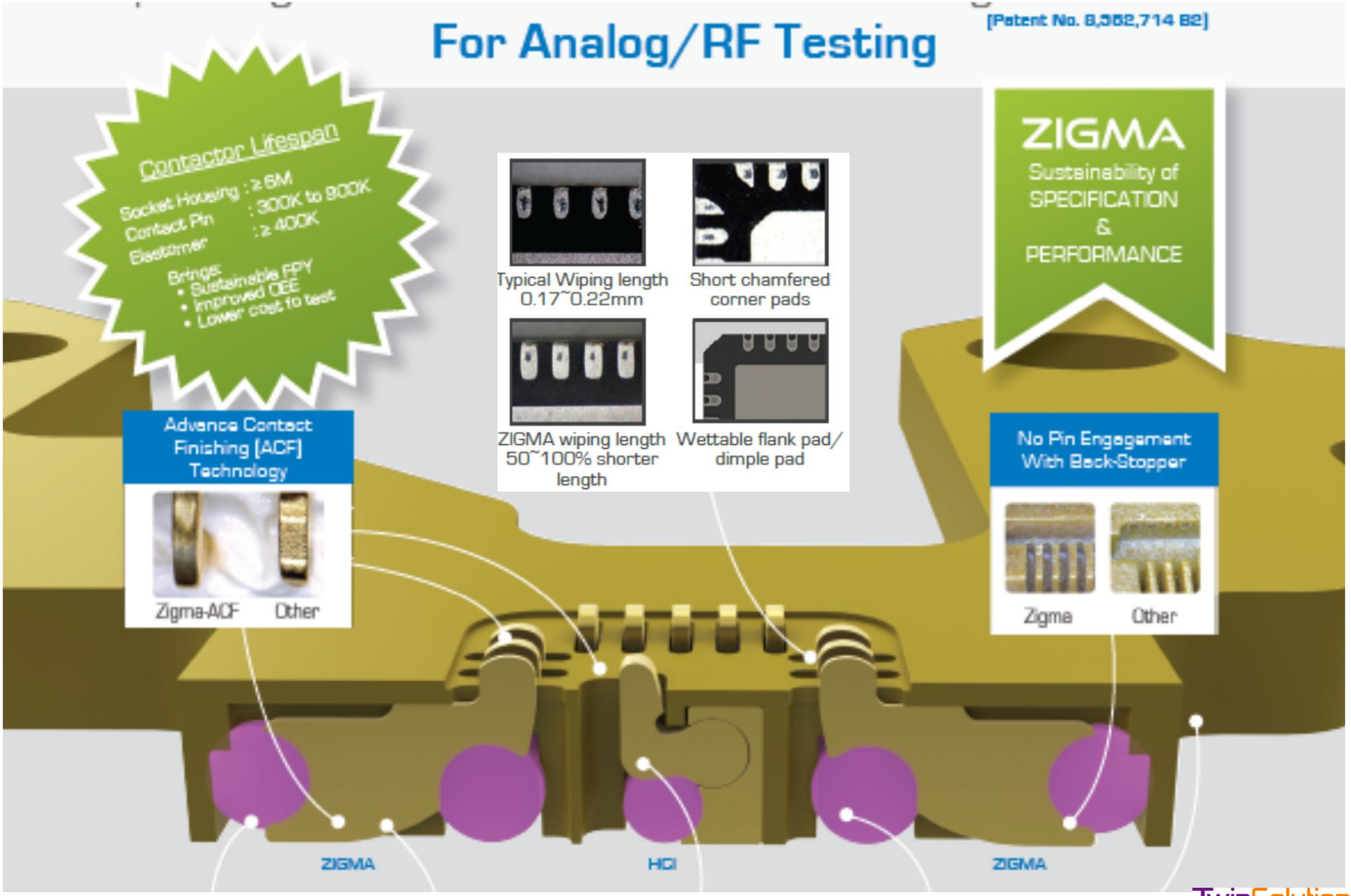
Signal Pin – Controlled 50ohm

Power Pin– Insulation Coating,

As close as possible to center grounding block, to provide less inductance

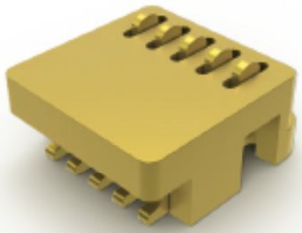
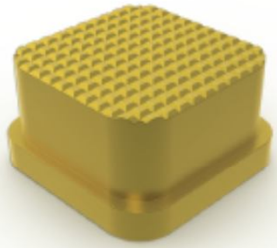
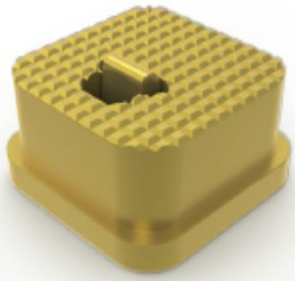
Ground Pin– Grounding,

Zigma1 – S Contactor for QFN

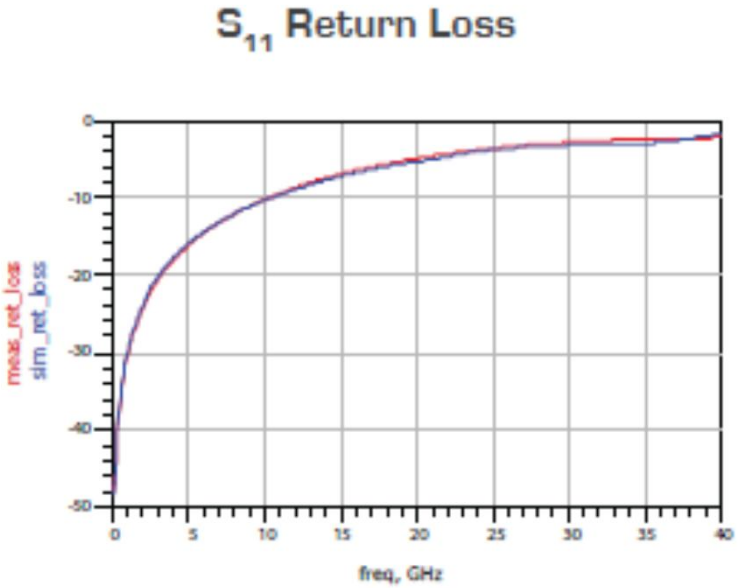


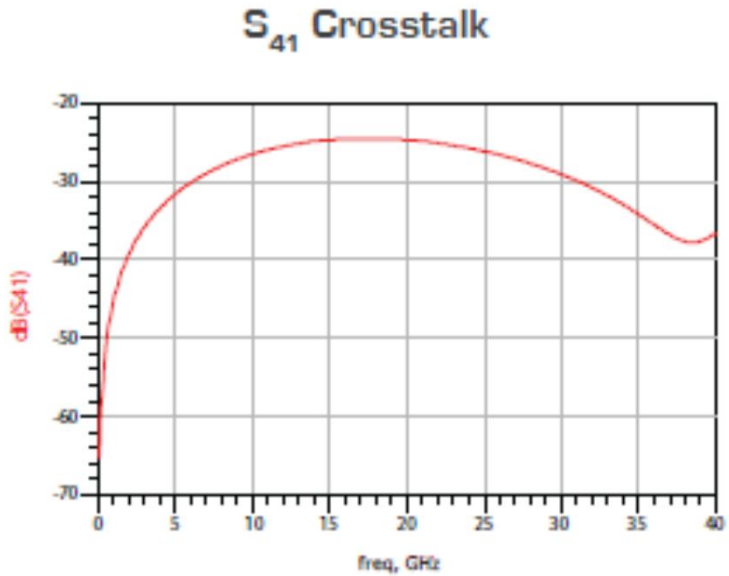
Zigma1 – S Contactor for QFN

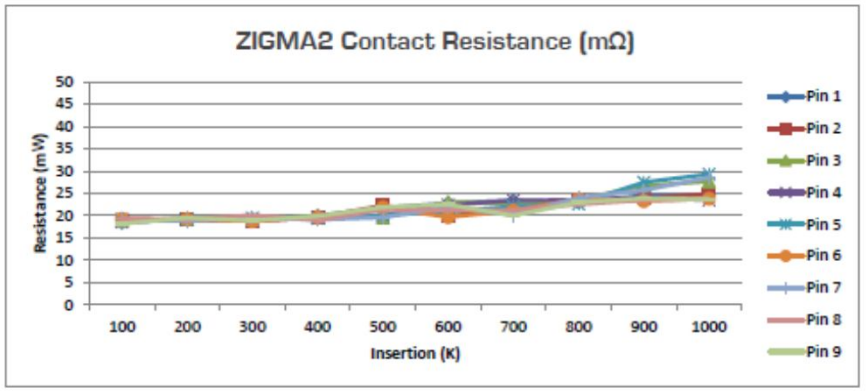
ZIGMA Grounding Pin Solutions			
Bell Contact (BC) [Patent Pending]	Hinged Contact Insert (HCI) [Patent Pending]	ZIGMA Short Pin (ZSP)	ZIGMA Pin (ZP)
			
For Package: ≥ 2x2	For Package: ≥ 3x3	For Package: ≥ 4x4	For Package: ≥ 5x5

ZIGMA Grounding Block Solutions			
Ground Block	Ground Block with Pin	Spike Ground Block	Spike Ground Block with Pin
			
For Package: ≥ 2x2	For Package: ≥ 3x3 (With HCI) ≥ 4x4 (With ZSP) ≥ 5x5 (With ZP)	For Package: ≥ 2x2	For Package: ≥ 3x3 (With HCI) ≥ 4x4 (With ZSP) ≥ 5x5 (With ZP)

Zigma1 – S Contactor for QFN



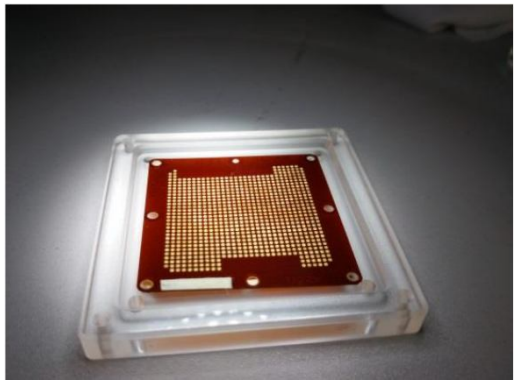


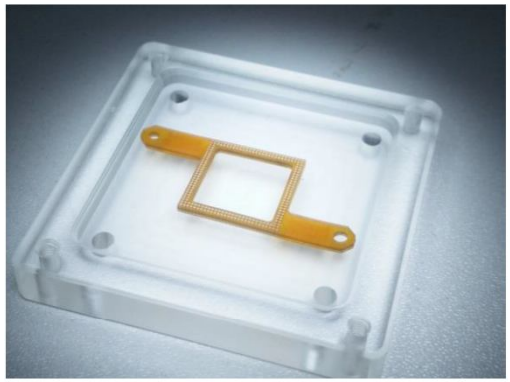


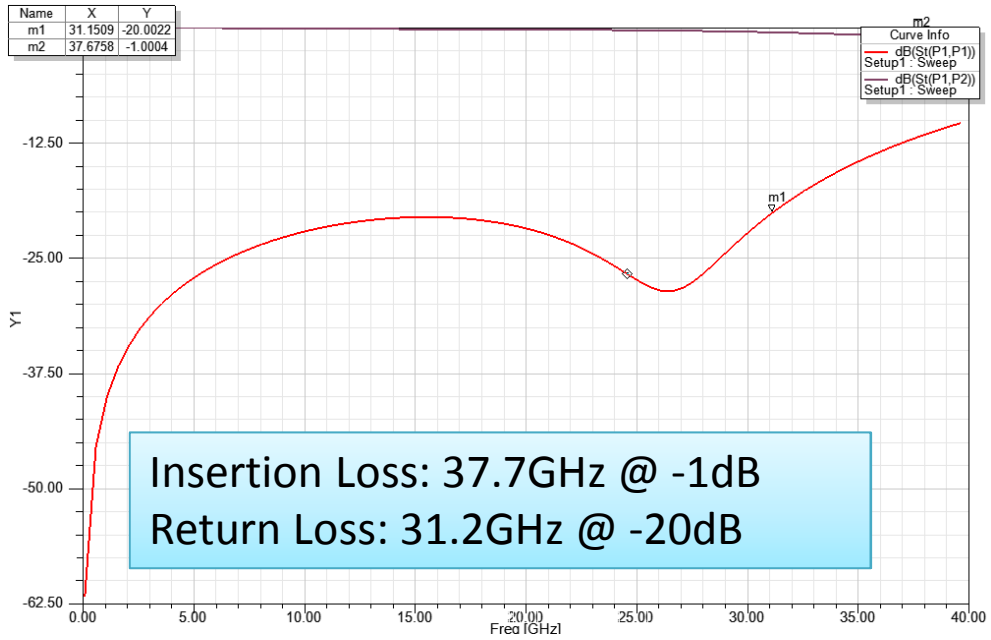
TwinSolution

Blade- Elastomer Contactor Socket

Socket Example

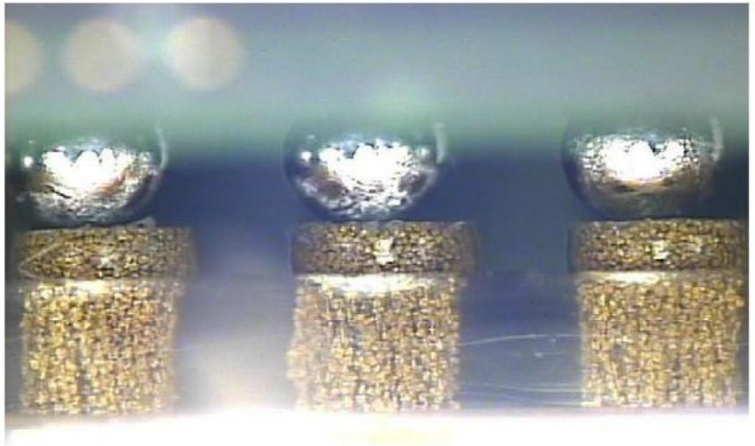




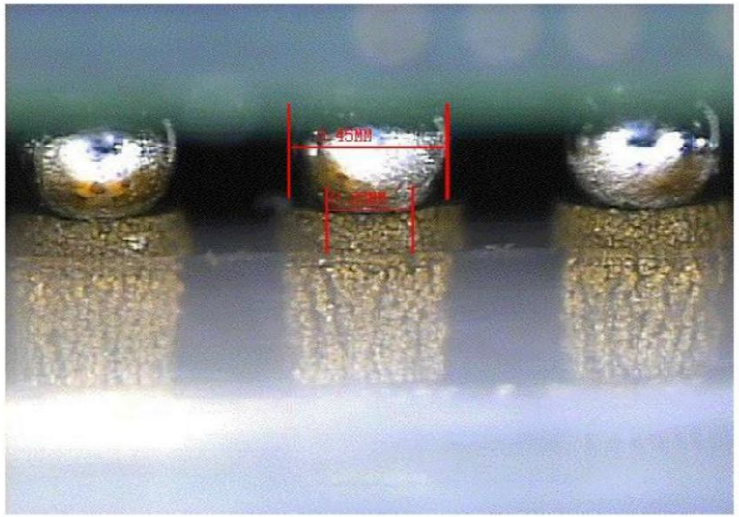


Insertion Loss: 37.7GHz @ -1dB
Return Loss: 31.2GHz @ -20dB

Before Contact

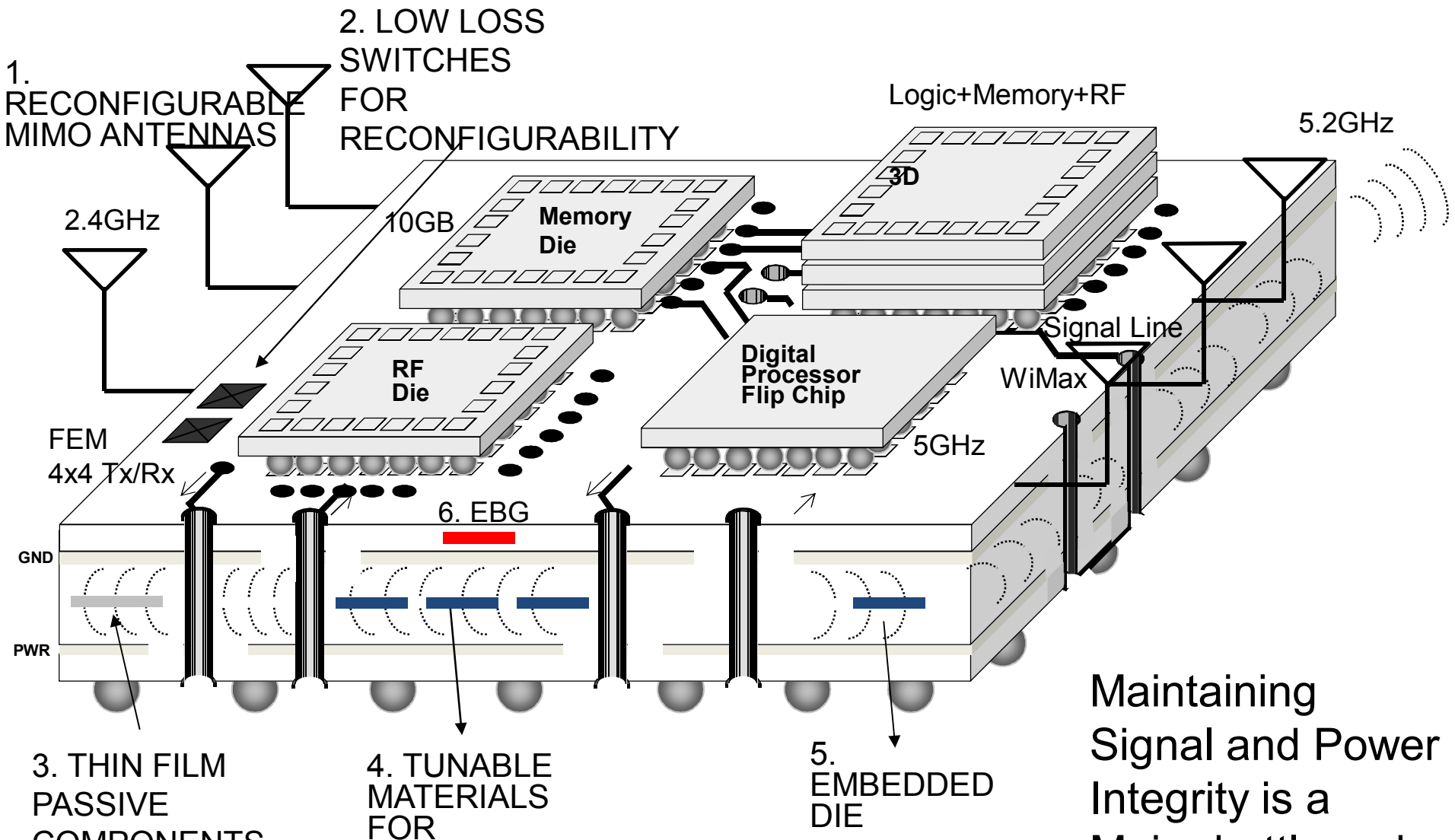


After Contact



Power Integrity

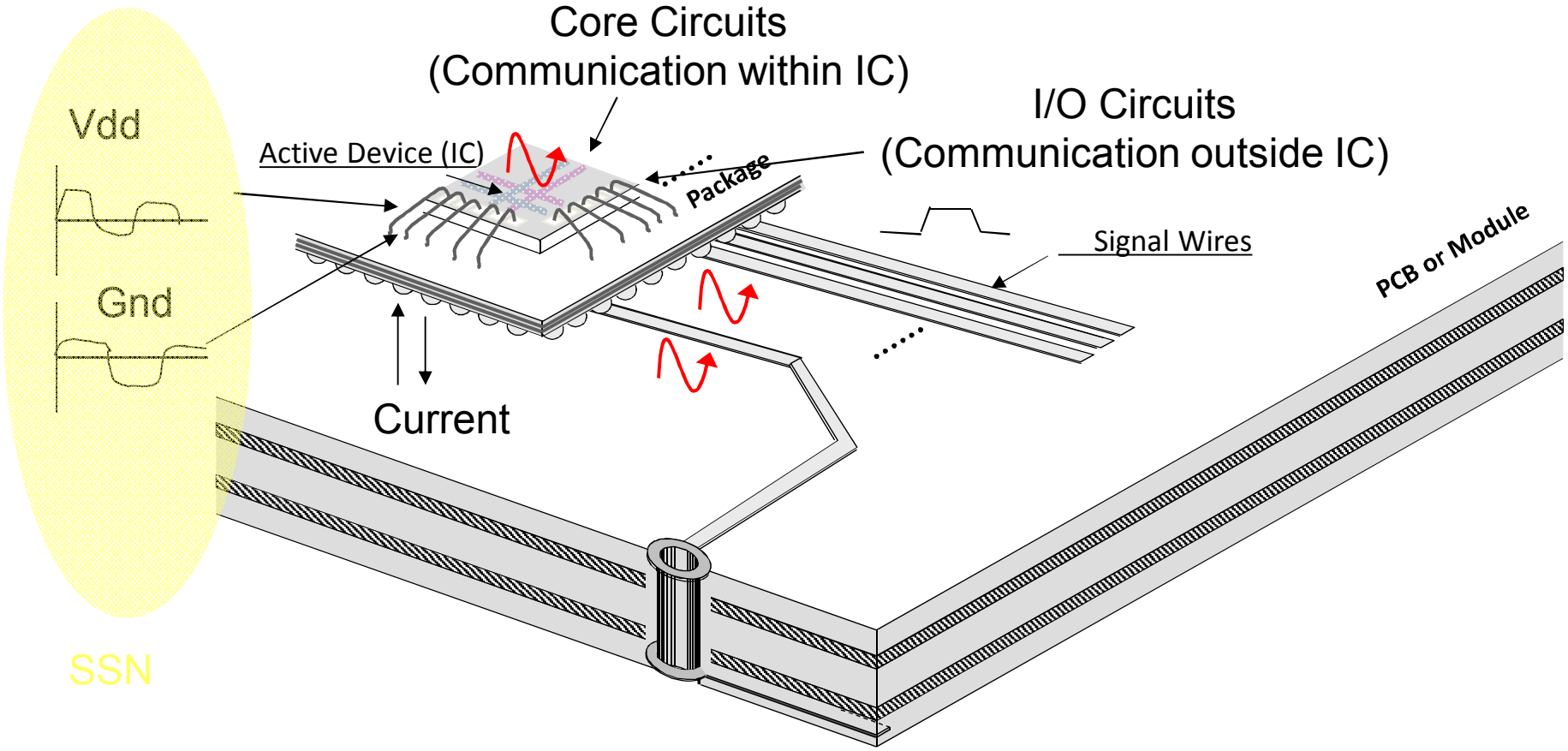
Ultra-Miniaturized Mobile Computing Platform



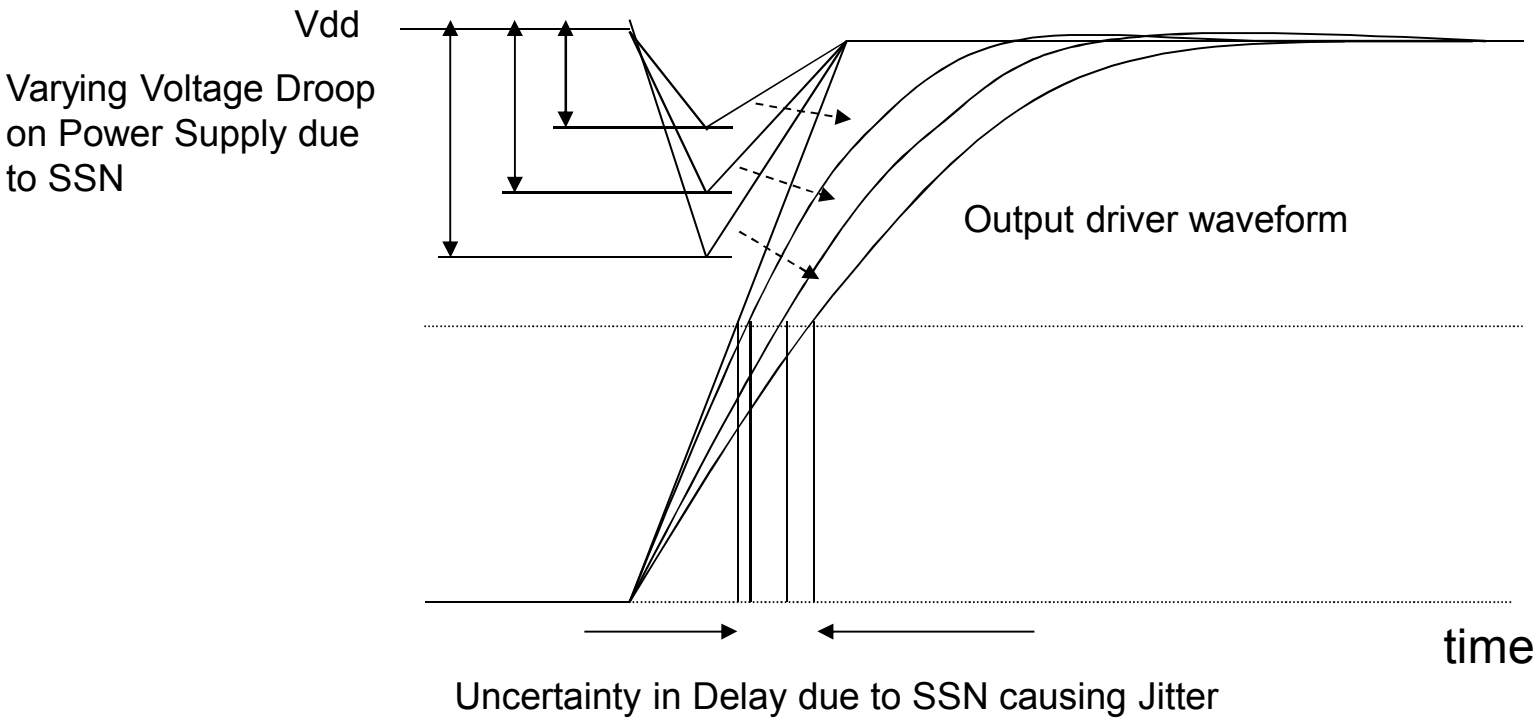
Maintaining Signal and Power Integrity is a Major bottleneck

TwinSolution

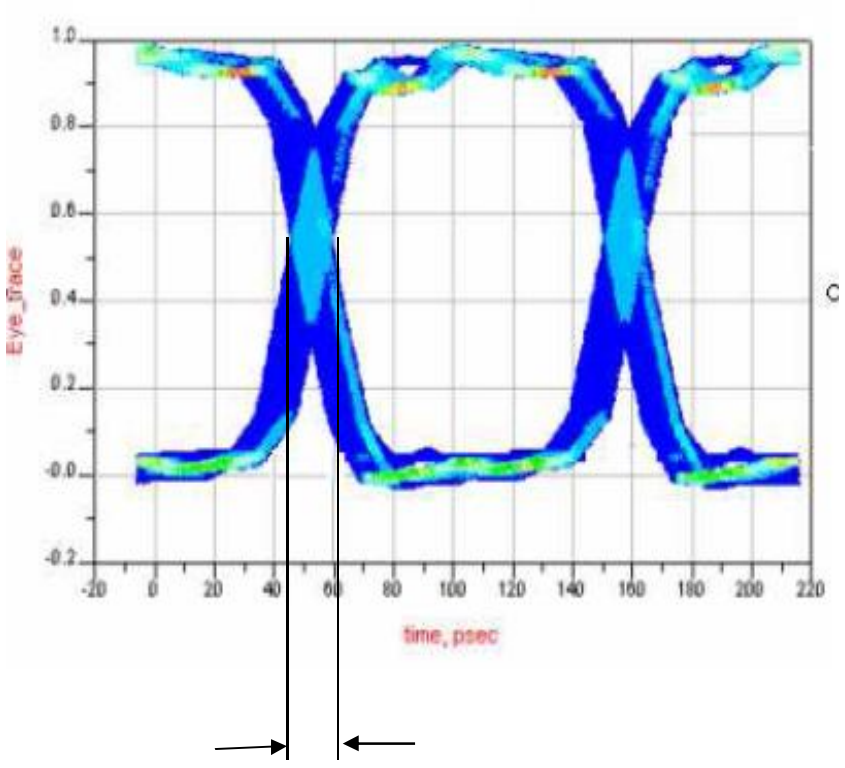
SSN in High-Speed / High-I/O Packages and High-Speed Boards



Jitter caused by SSN for I/O

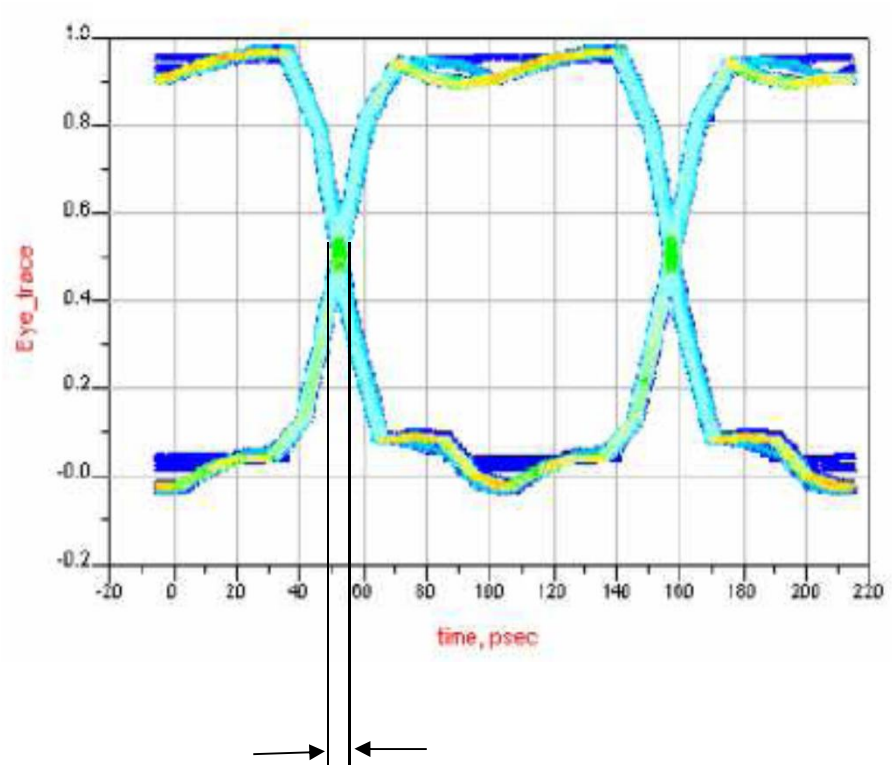


SSN affects Jitter



Jitter = 18 ps

50um thick dielectric

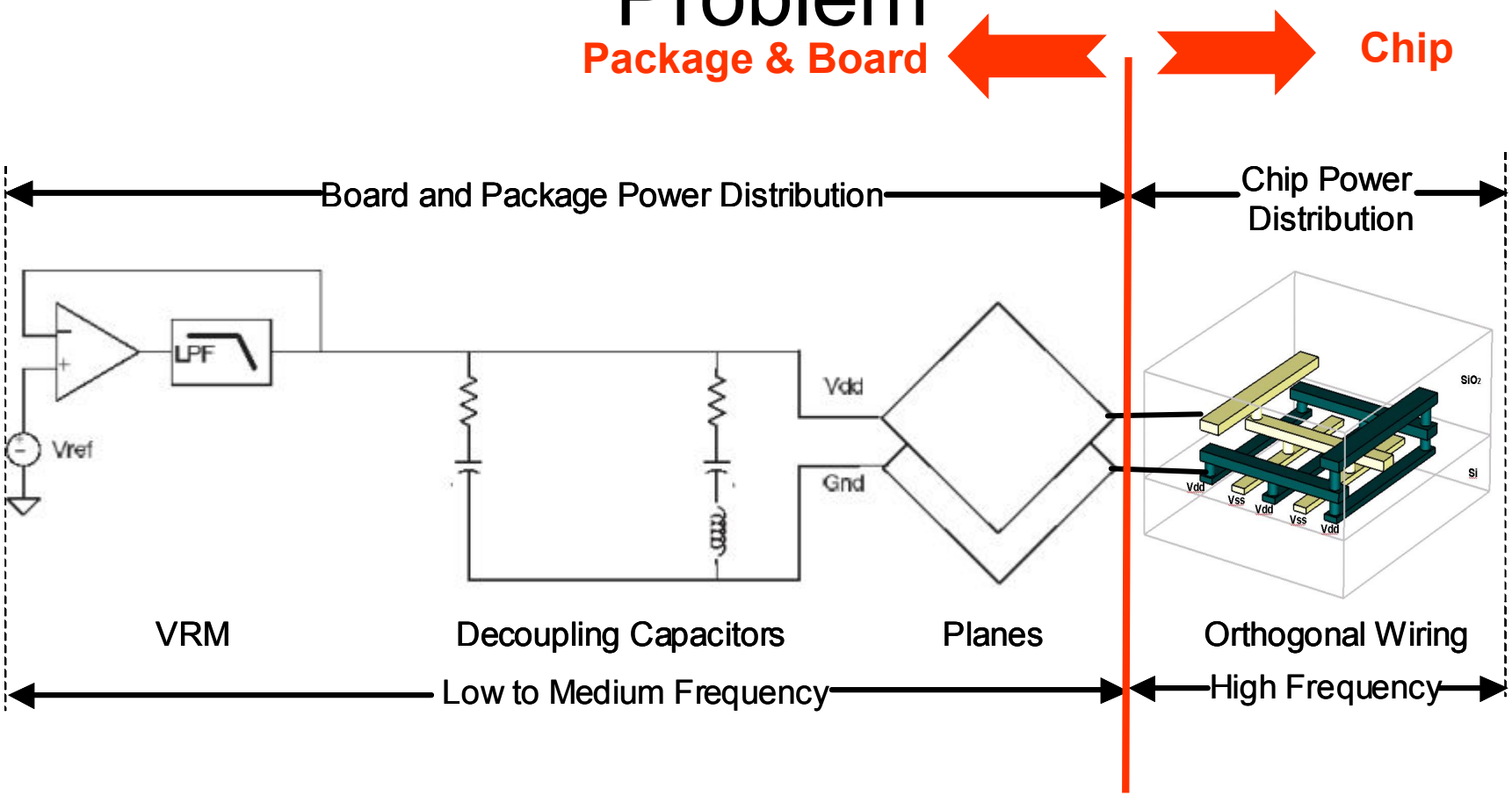


Jitter = 8 ps

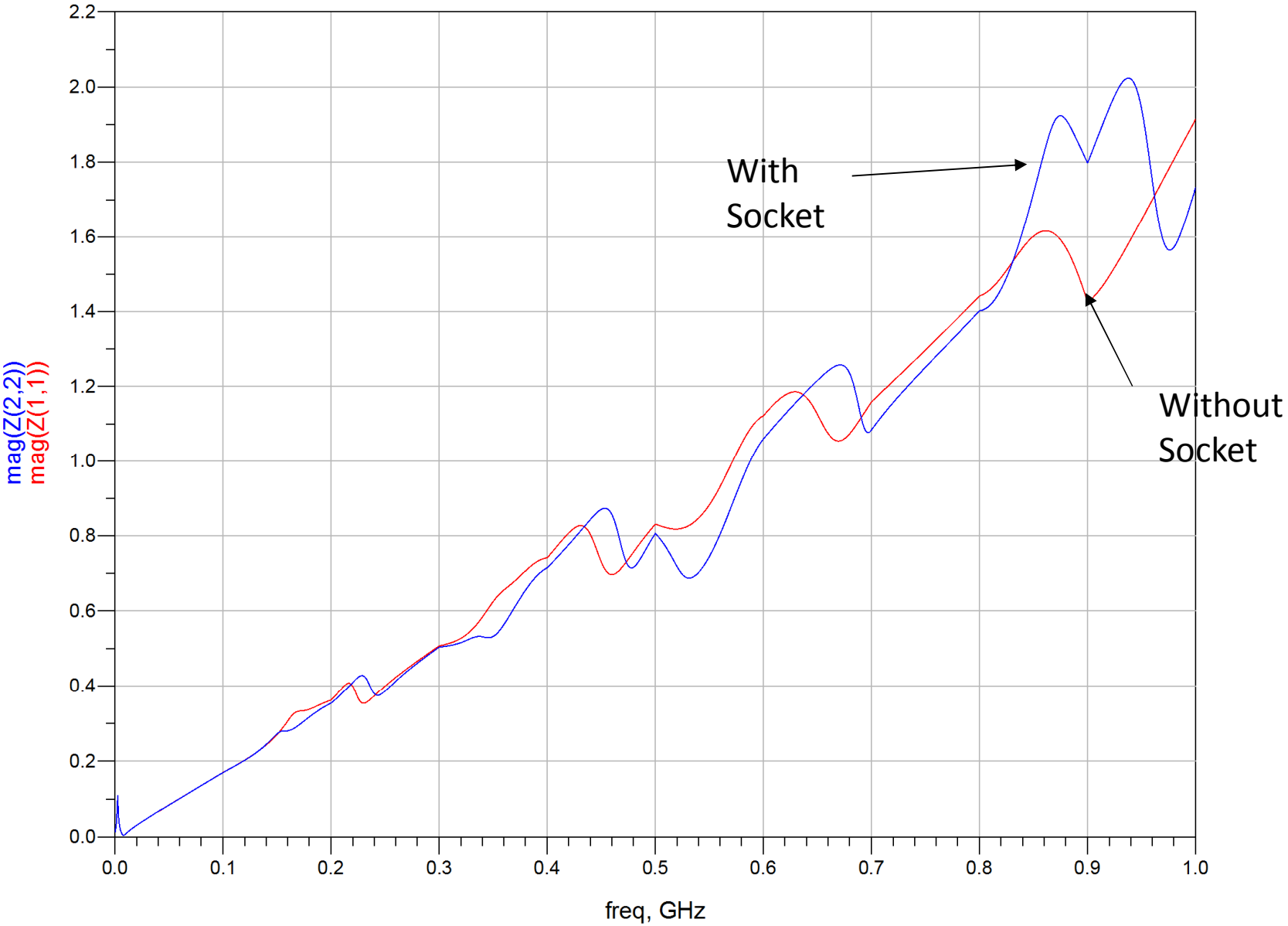
18um thick dielectric

PDN Impedance affects jitter in high speed signaling

Power Distribution – DC to Daylight Problem

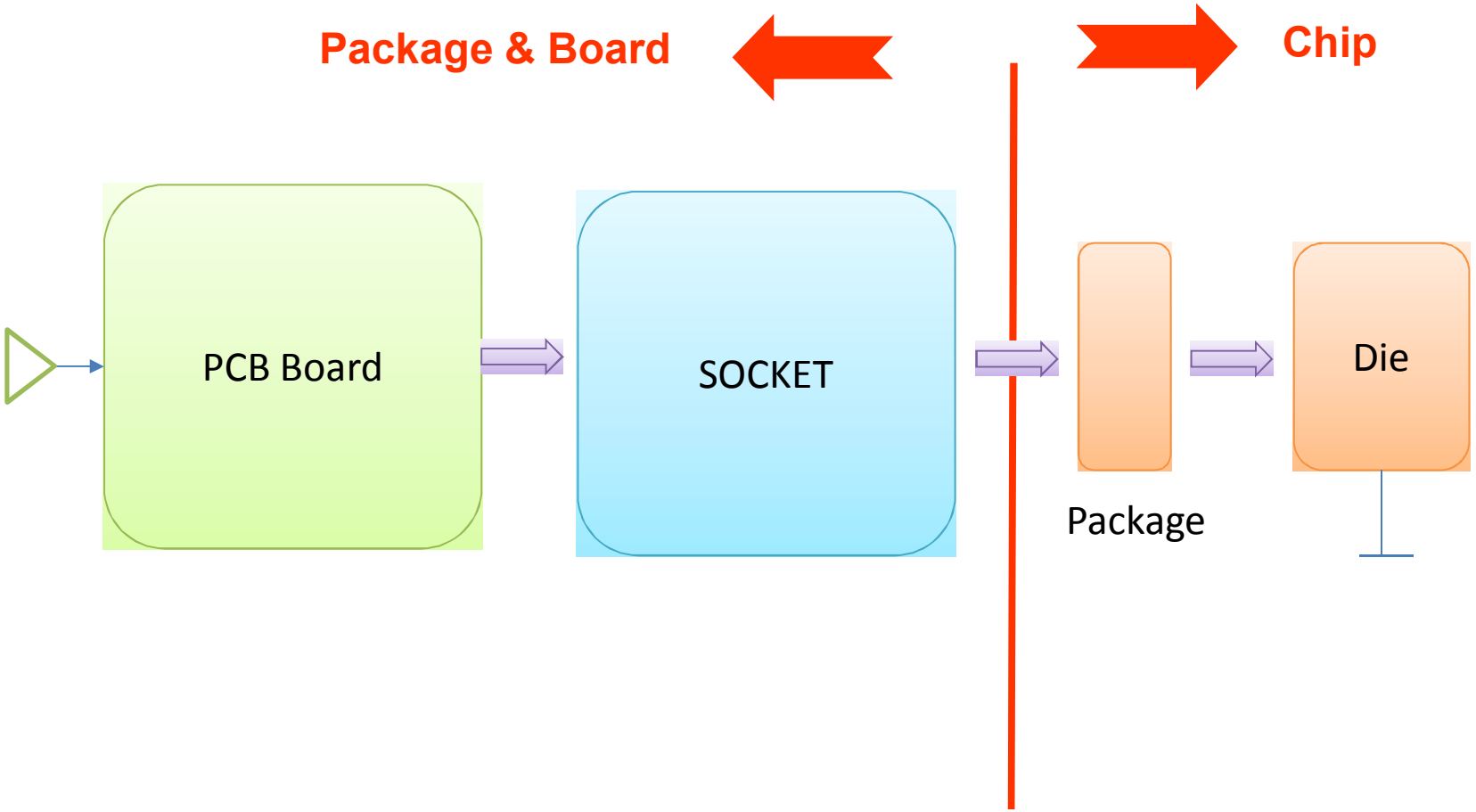


Chip – Package Co-design of Power Distribution necessary for high performance systems

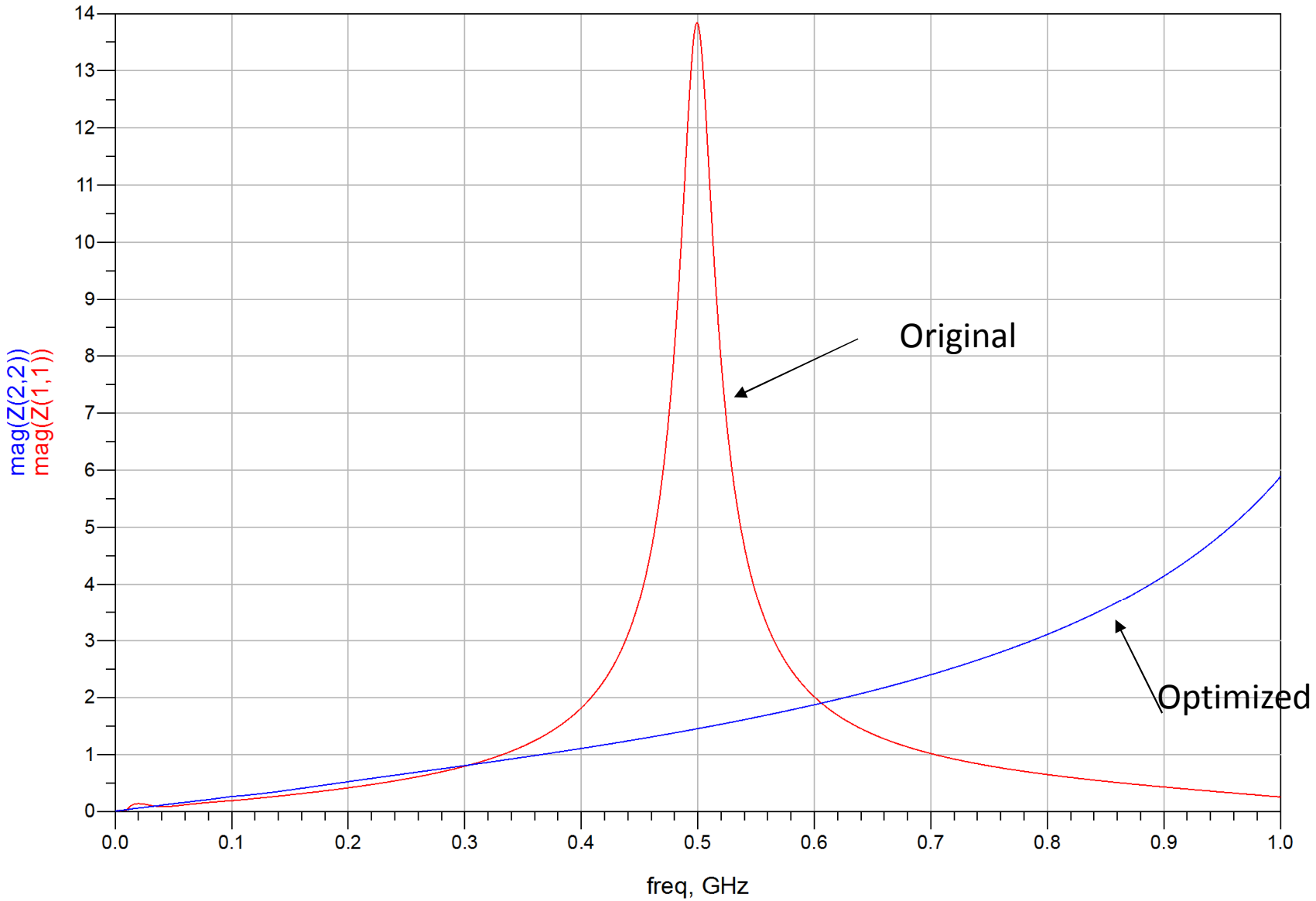


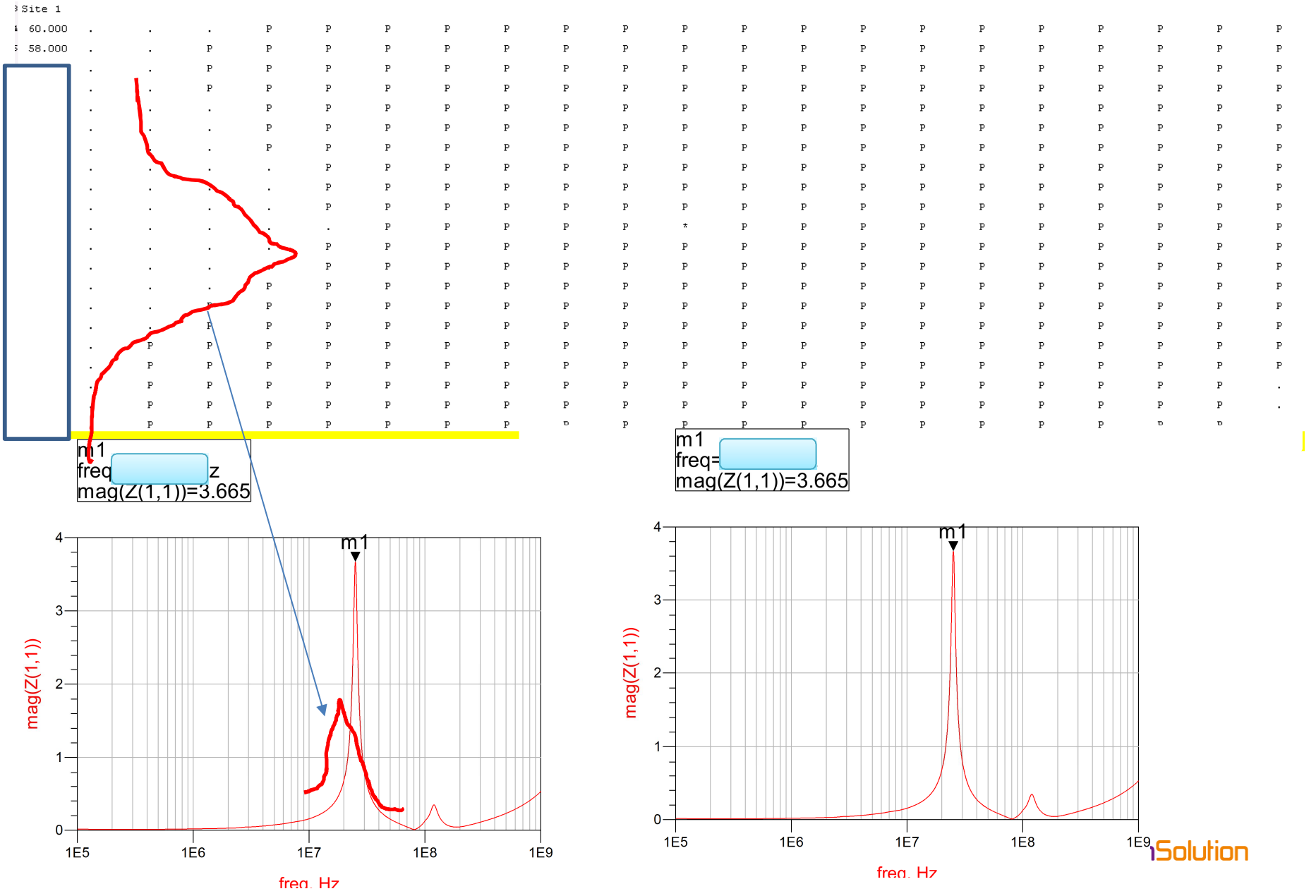
TwinSolution

Power Distribution



Chip – Package Co-design of Power Distribution necessary for high performance systems




Site 1
60.000
58.000
m1
freq z
mag(Z(1,1))=3.665
m1
freq=
mag(Z(1,1))=3.665
m1
mag(Z(1,1))
4
3
2
1
0
1E5
1E6
1E7
1E8
1E9
freq, Hz
m1
mag(Z(1,1))
4
3
2
1
0
1E5
1E6
1E7
1E8
1E9
freq, Hz
Solution

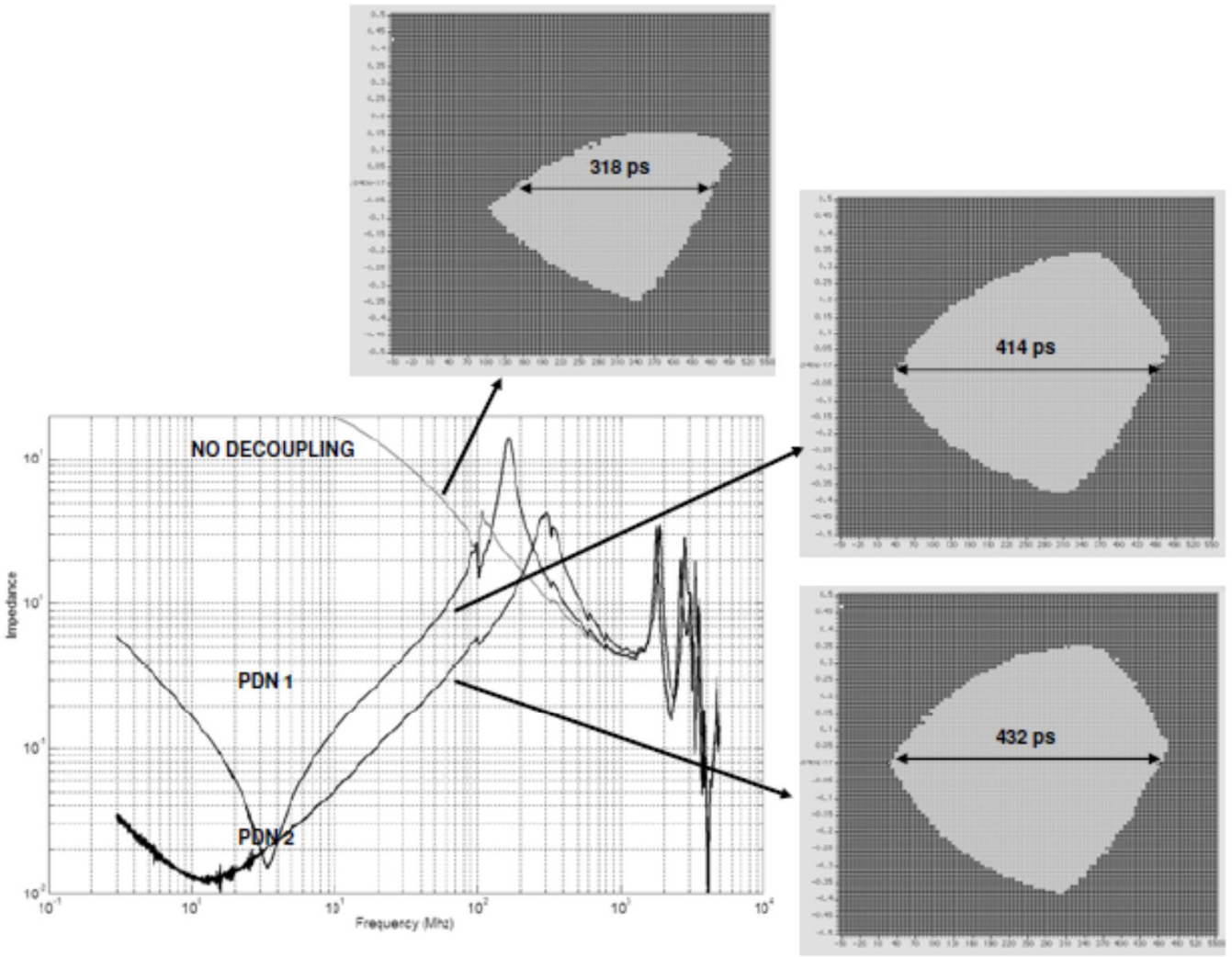
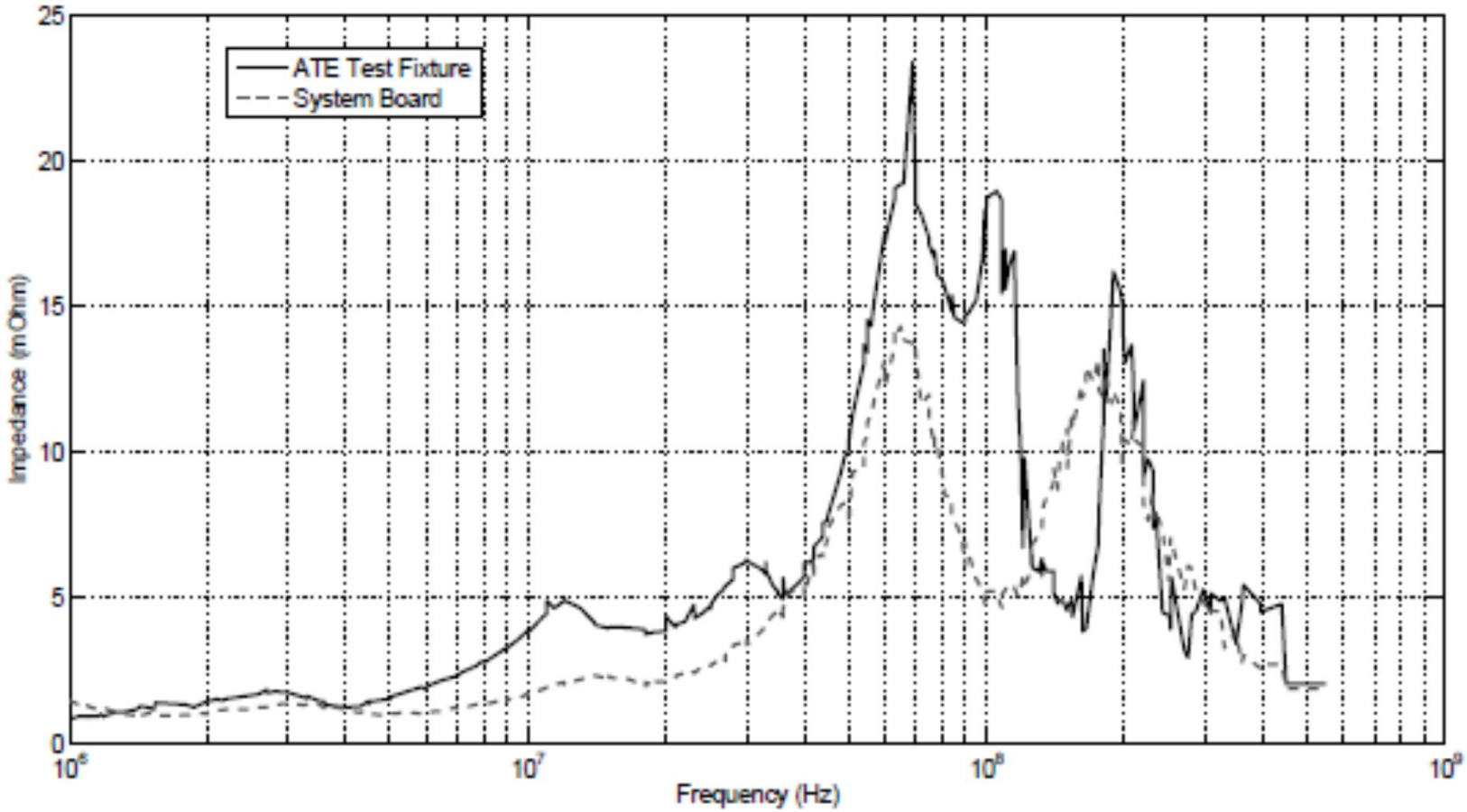
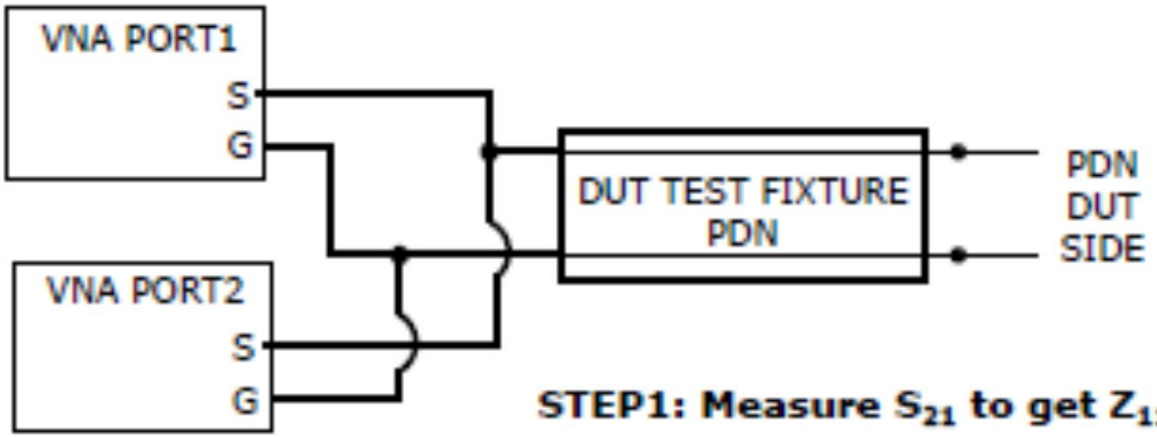


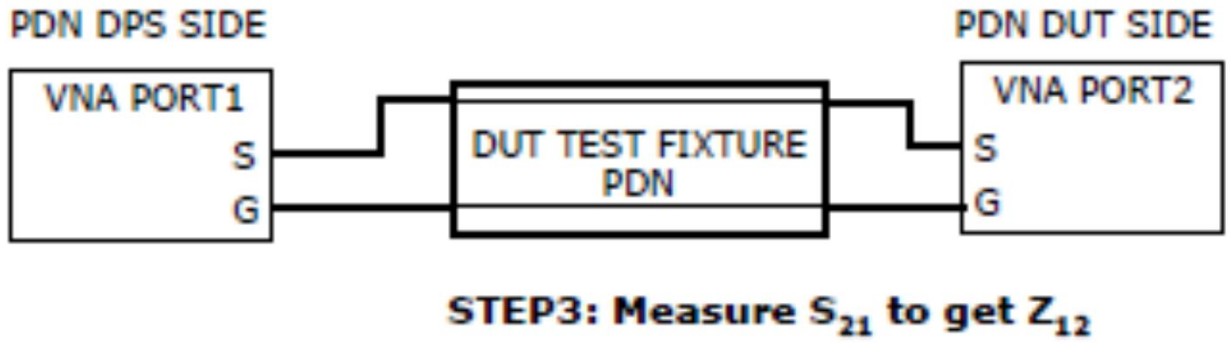
Figure 8.66 Comparison of the effect of different test fixture PDN designs on the data eye from a DQ pin of a DDR3 memory running at 1.6 Gbps.

Are you OK with your SHMOO?



Power Impedance Measurement

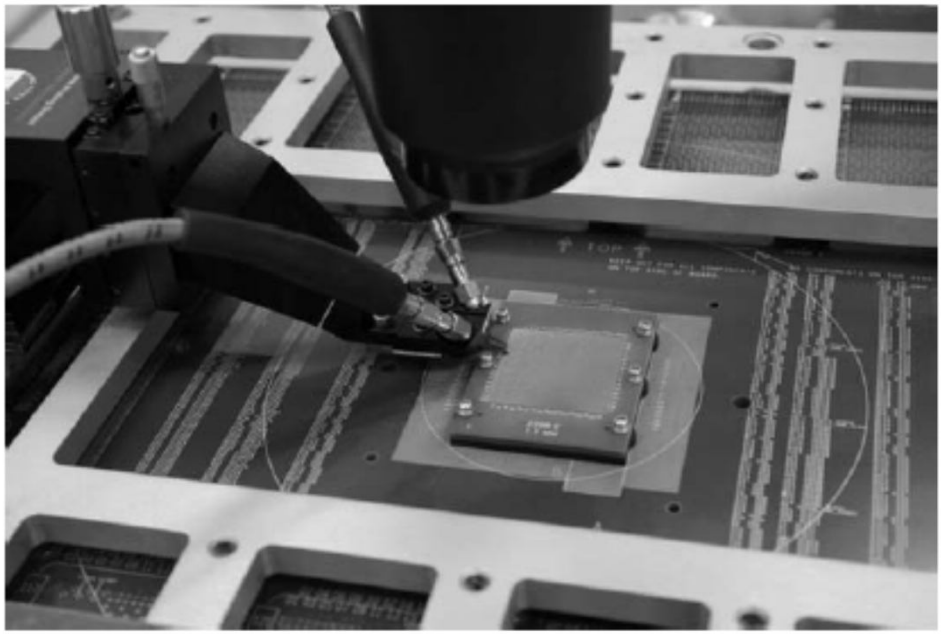




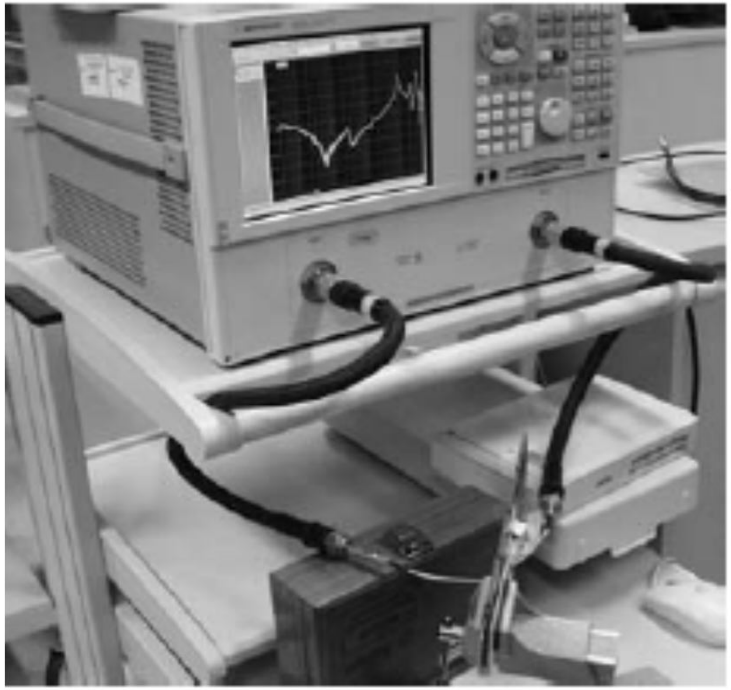
Power Impedance Measurement

$$
\begin{aligned}
Z_{11} &= \frac{Z_{\mathrm{VNA}}}{2}\,\frac{S_{21}^{(1)}}{1-S_{21}^{(1)}} \\
Z_{22} &= \frac{Z_{\mathrm{VNA}}}{2}\,\frac{S_{21}^{(2)}}{1-S_{21}^{(2)}} \\
Z_{12} = Z_{21} &= \frac{Z_{\mathrm{VNA}}}{2}\,S_{21}^{(3)}\,\frac{1+\frac{Z_{11}}{Z_{\mathrm{VNA}}}+\frac{Z_{22}}{Z_{\mathrm{VNA}}}+\frac{Z_{11}}{Z_{\mathrm{VNA}}}\frac{Z_{22}}{Z_{\mathrm{VNA}}}}{1+S_{21}^{(3)}\frac{Z_{11}}{2Z_{\mathrm{VNA}}}}
\end{aligned}
\qquad \text{(H.1)}
$$

Power Impedance Measurement



(c) Using a probe together with an interposer to measure the test fixture performance including the DUT socket.



network measurement setups (left:
Z_{12}).

ADC Load Board

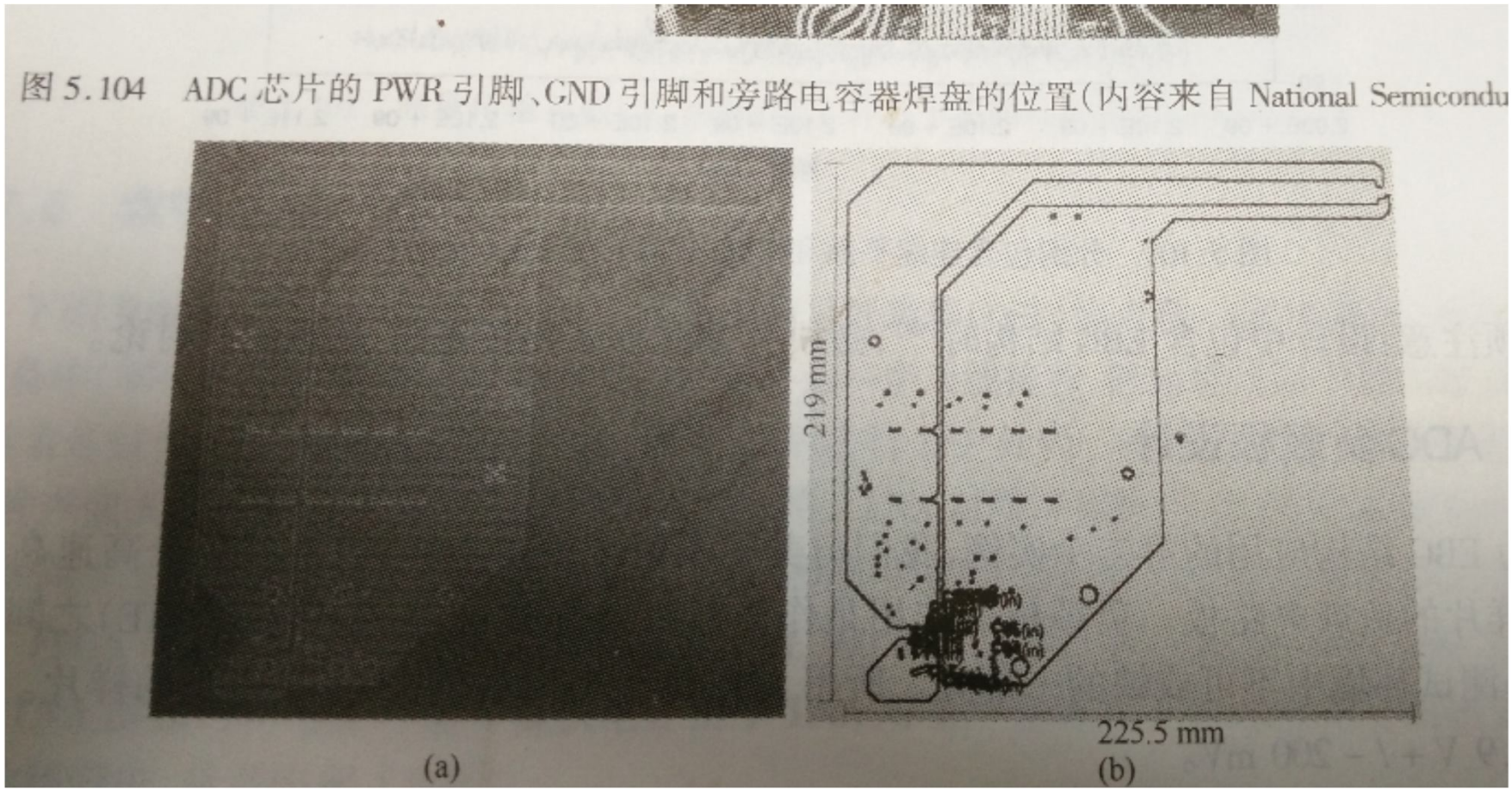


图 5.104　ADC 芯片的 PWR 引脚、GND 引脚和旁路电容器焊盘的位置(内容来自 National Semicondu

ADC Load Board- Correction

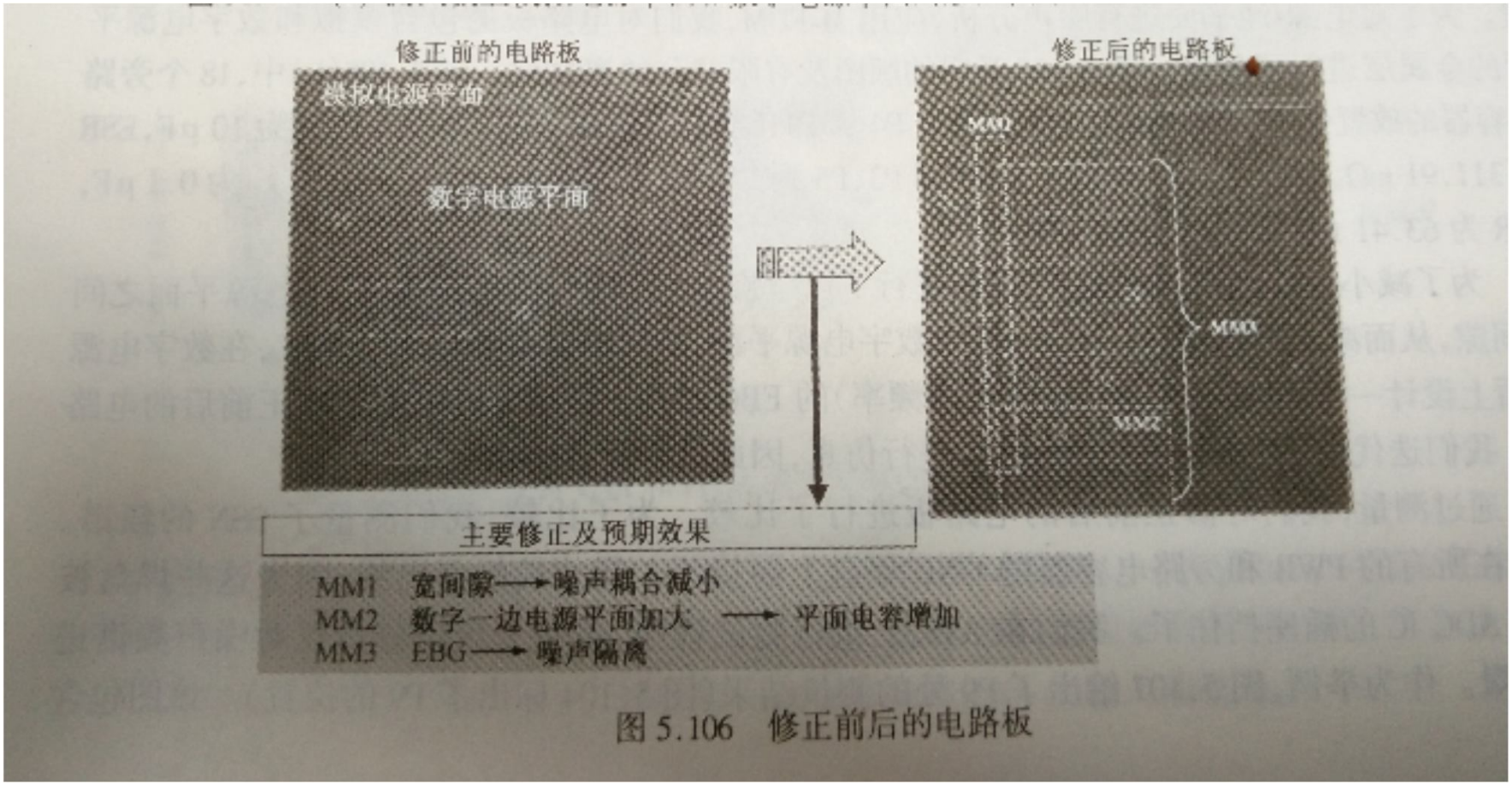


图 5.106 修正前后的电路板

Result

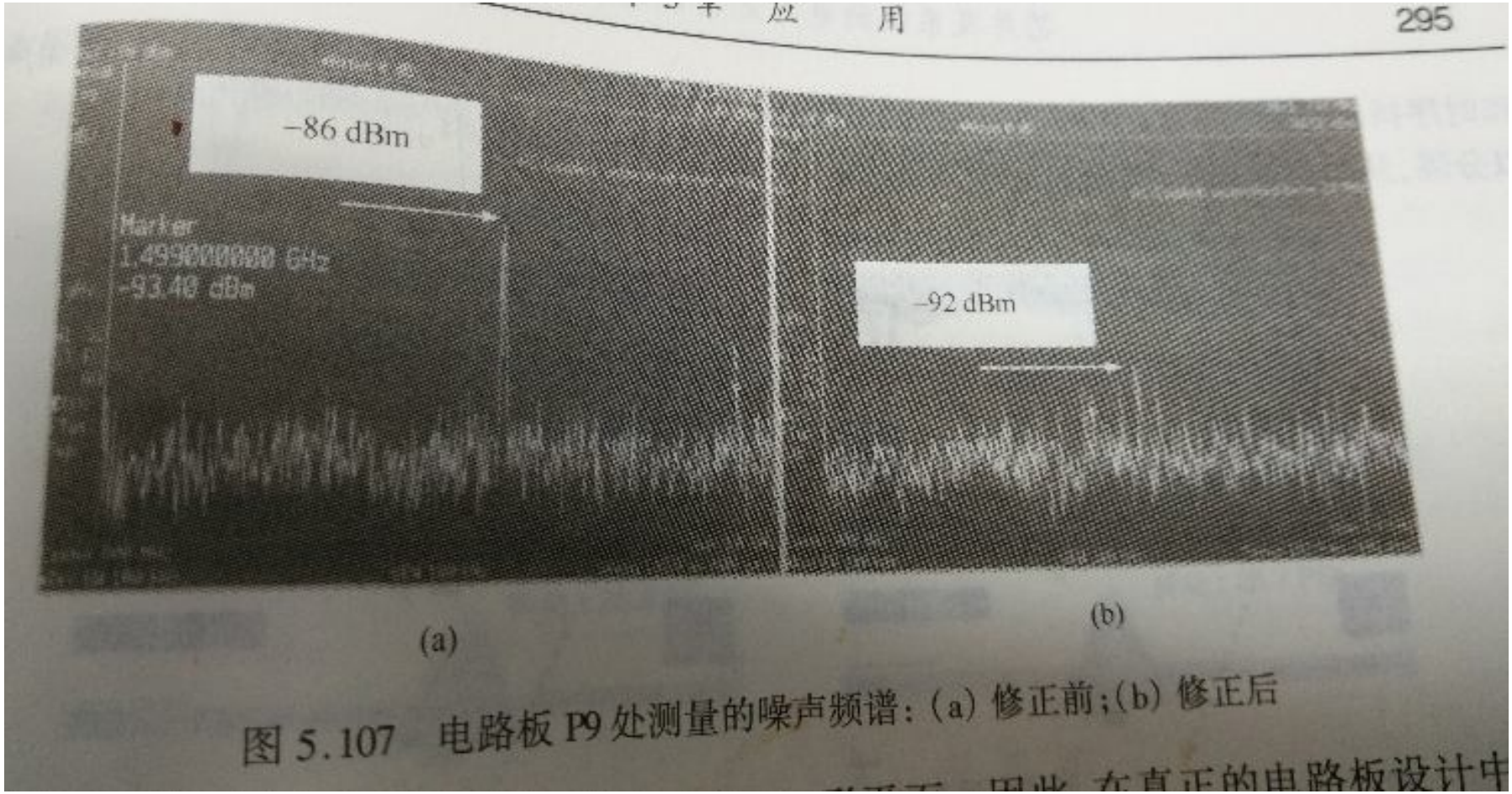
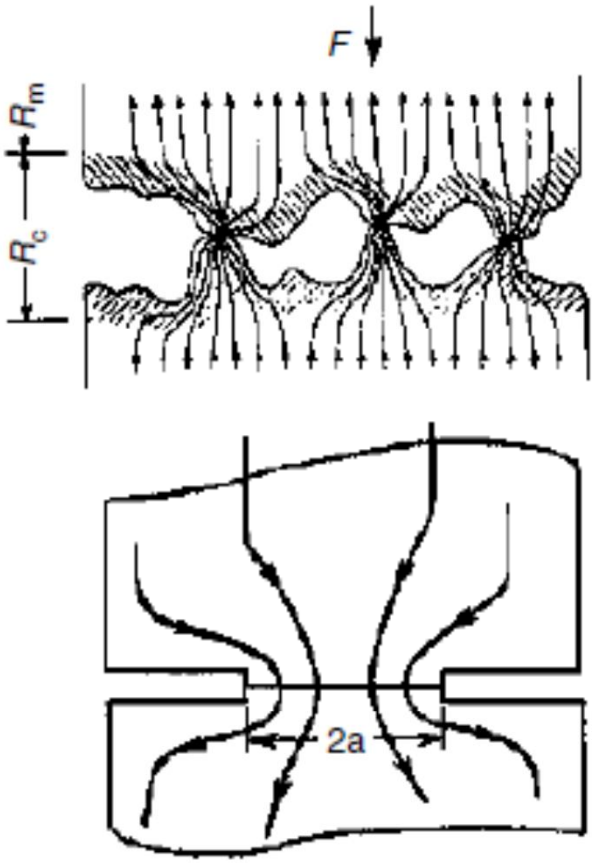
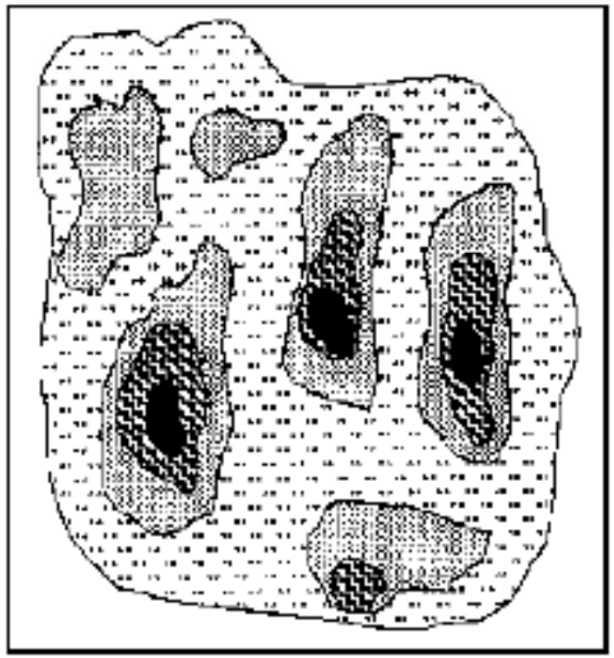


图 5.107　电路板 P9 处测量的噪声频谱：(a) 修正前；(b) 修正后

$$Z = \underline{R} + jX$$



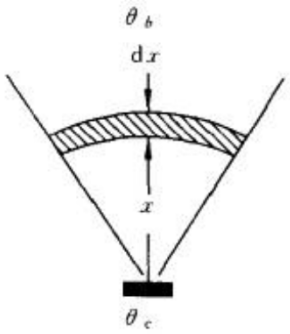
R_m Conductor resistance
R_c Constriction resistance
a Diameter of a-spot



Apparent (nominal) contact area
Real contact area
Load-bearing area
Quasi-metallic contact area
Conducting contact area (a-spots)

$$F_{\mathrm{c}} = \xi H A_{\mathrm{a}}$$

Contact Point Temperature Difference



$$-\mathrm{d}\theta = (I^2R)\cdot \mathrm{d}R_t = I^2R\cdot\frac{1}{\rho\lambda}\cdot \mathrm{d}R$$

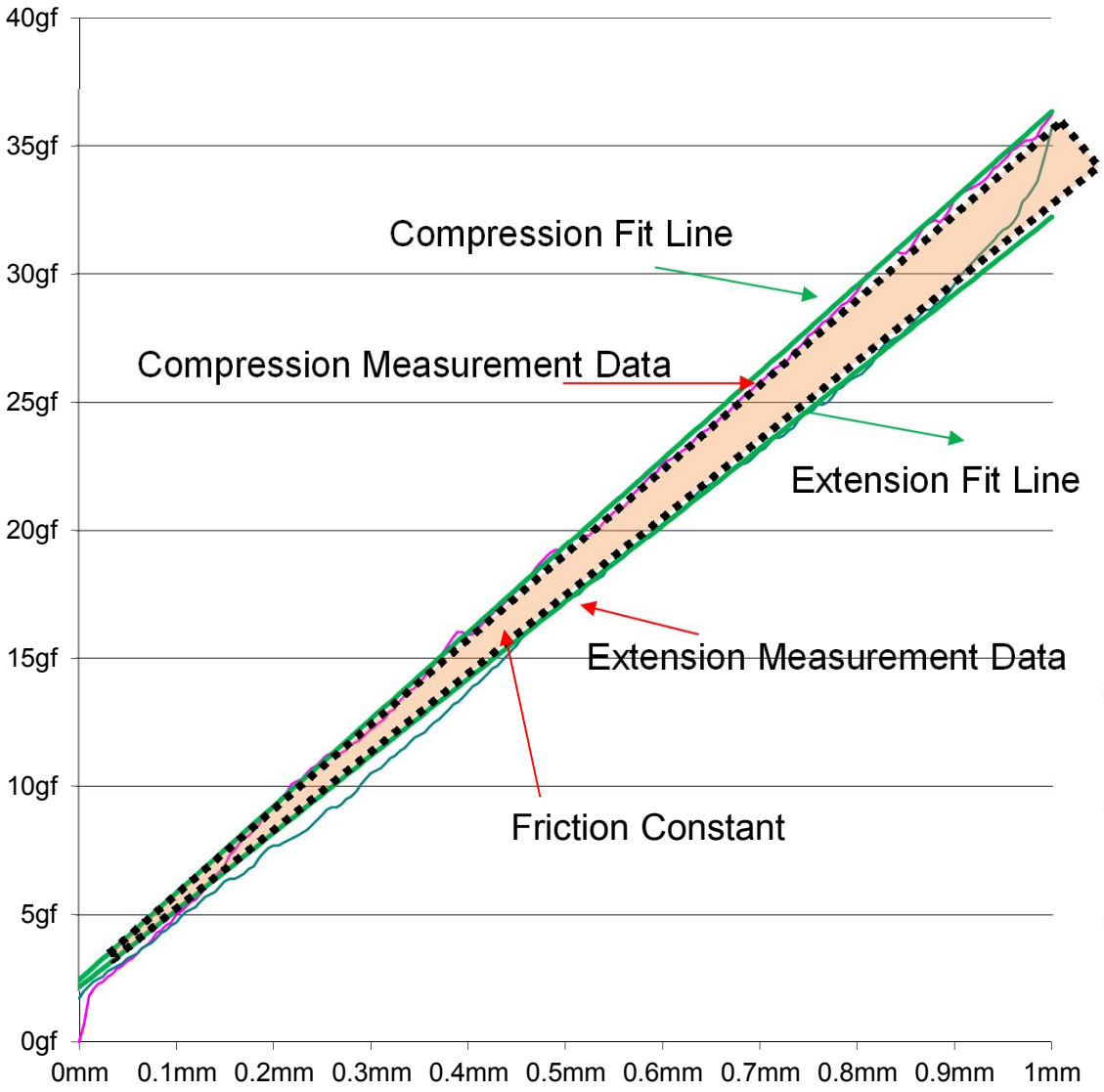
$$\int_{\theta_c}^{\theta_b} -\mathrm{d}\theta = \frac{I^2}{\rho\lambda}\int_0^{\frac{R_c}{2}} R\mathrm{d}R$$

$$\tau_c = \theta_c - \theta_b = \frac{I^2R_c^2}{8\lambda\rho} = \frac{U_c^2}{8\lambda\rho}$$

$$\tau_c = \frac{I^2R_c^2}{8LT} = \frac{U_c^2}{8LT}$$

Spring Pin Contact Resistance

Side Load Algorithm



Compression

$$fc(x) = (1+u) * f_0 + \left(1 + u * \frac{lg}{\frac{ls}{2} - x_c}\right) * \mathrm{K} * x_c$$

Extension

$$fe(x) = (1-u) * f_0 + \left(1 - u * \frac{lg}{\frac{ls}{2} - x_e}\right) * \mathrm{K} * x_e$$

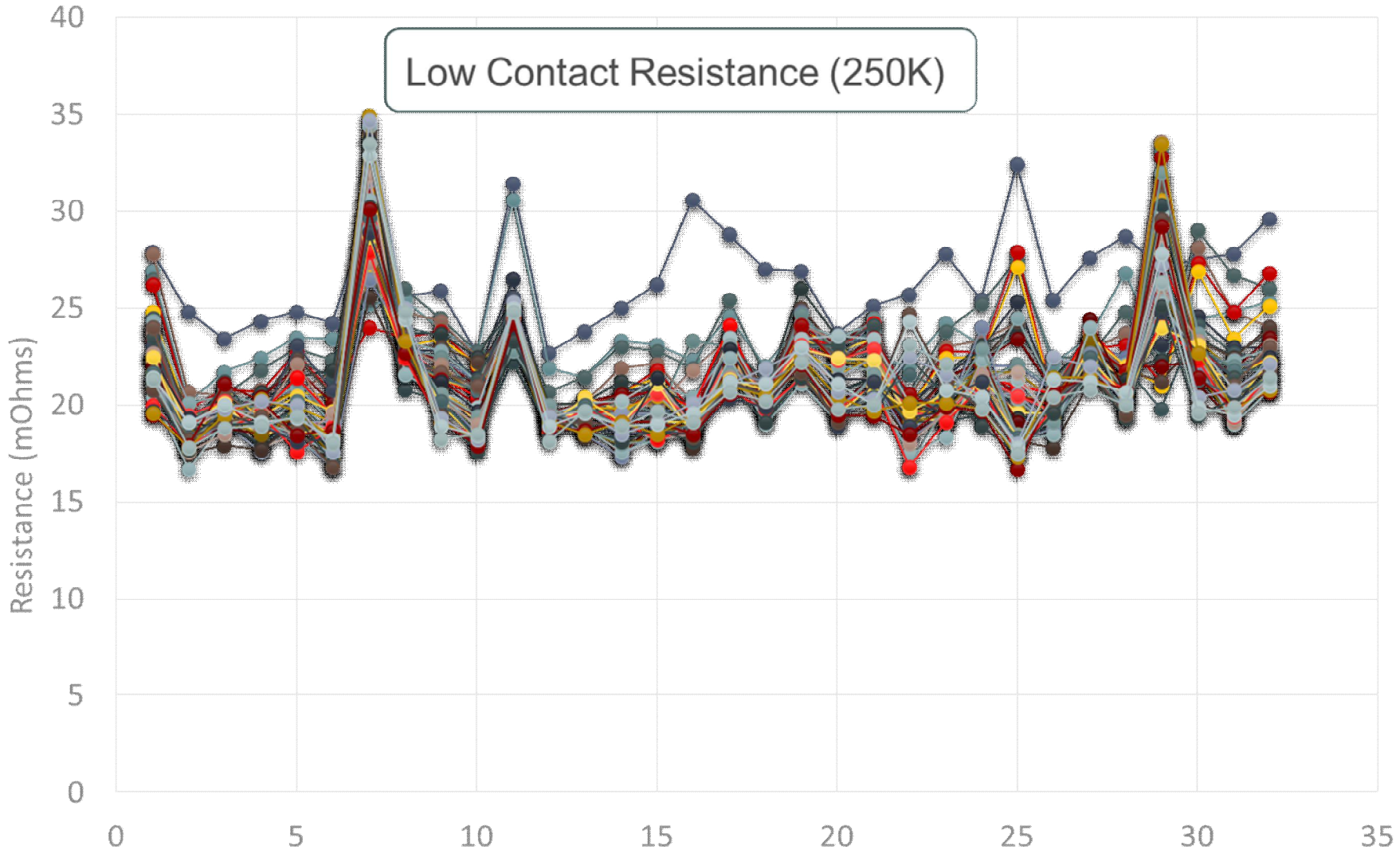
$u =$ Frictional Constant

$f_0 =$ Preload Force

$K =$ Spring Constant

- Side force is impacting the total spring force,
- Side force provide the robust contact of the slid bearing.
- By using the algorithm, we are able to determine whether the pin is designed a good contact situation.

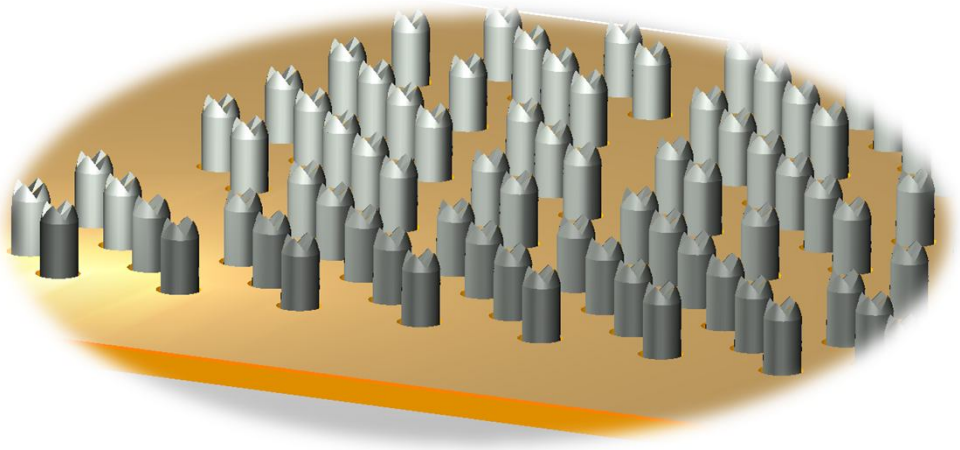
TwinSolution

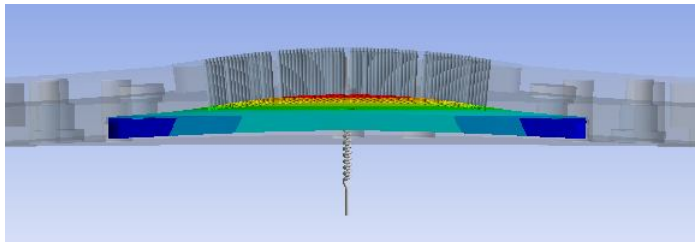


TwinSolution

Firefly– WLCSP Probe Head

- Pitch 400um
- Pin Length: 2.4mm
- Device: 3GHz
- Sites: 8
- Pin count: 960
- Optimize to minimum deflection of PCB board.
- Status:
  - ✓ Customer Mass Production





FireFly: Case Study

Probe Head Electrical Performance Benchmark

High Power Mode

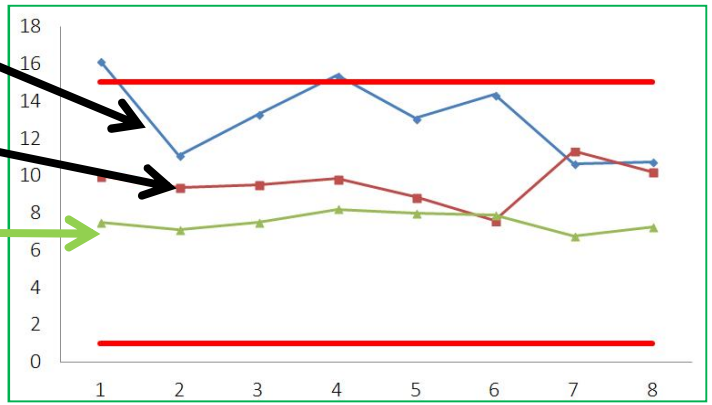
BT_TxDEVM_RMS_8DPSK_39

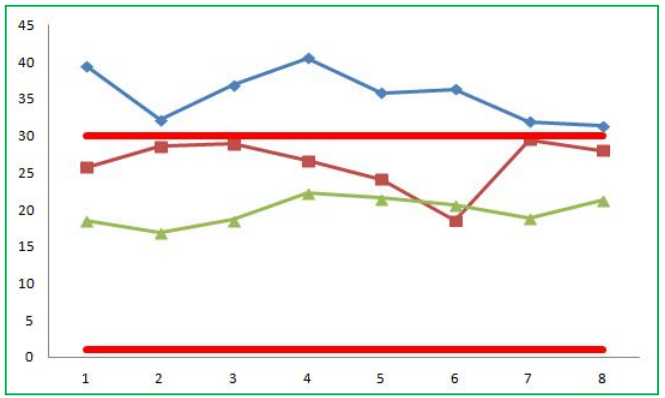
BT_TxDEVM_PK_8DPSK_39

Supplier I

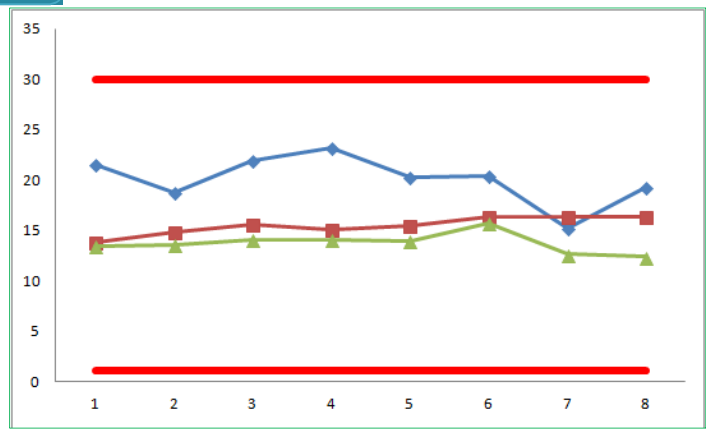
Supplier W

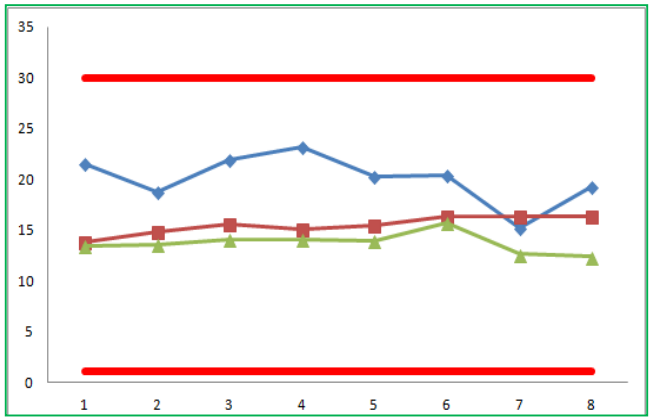
Twin -250Pin





Lower Power Mode

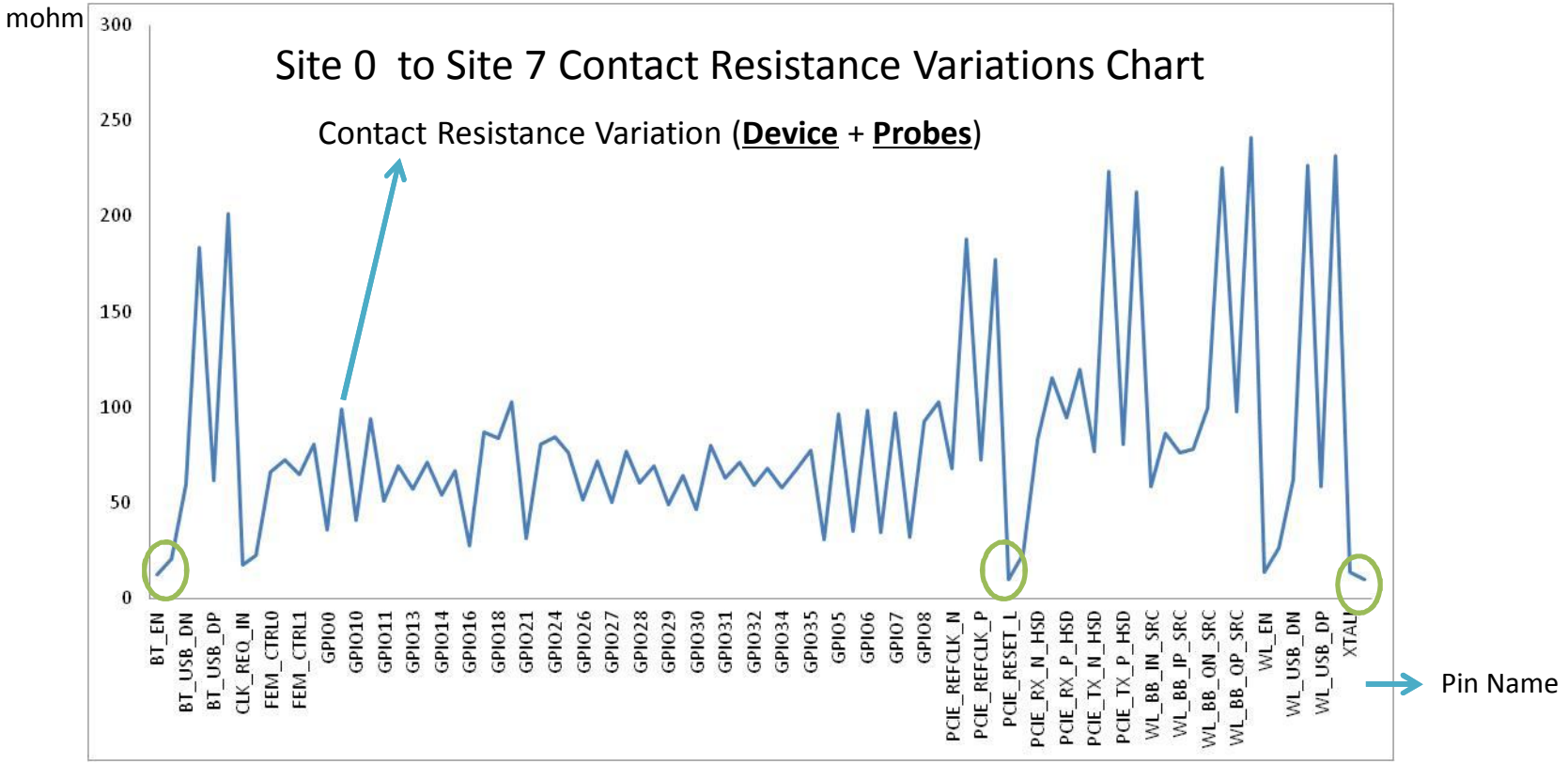




TwinSolution

FireFly : Case Study

Mechanical Performance - DC Continuity Test



- The minimum contact resistance variation from site0 to site7 is pin XTALO, and the contact resistance variation is 9.8mohm. This can consider the pure spring probe's contact resistance variation.
- The maximum variations happens to pin WL_BB_QP_SRC, it is around 240mohm, which should be also related to the device itself.