

Automotive TFQ

A brief introduction of automotive test for quality
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Why do we need this?

- Its quite simple – quality in automotive safety applications is critical, automotive OEM require **0 DPPM (Defective Parts Per Million)**.



Automotive Analog TFQ Methods

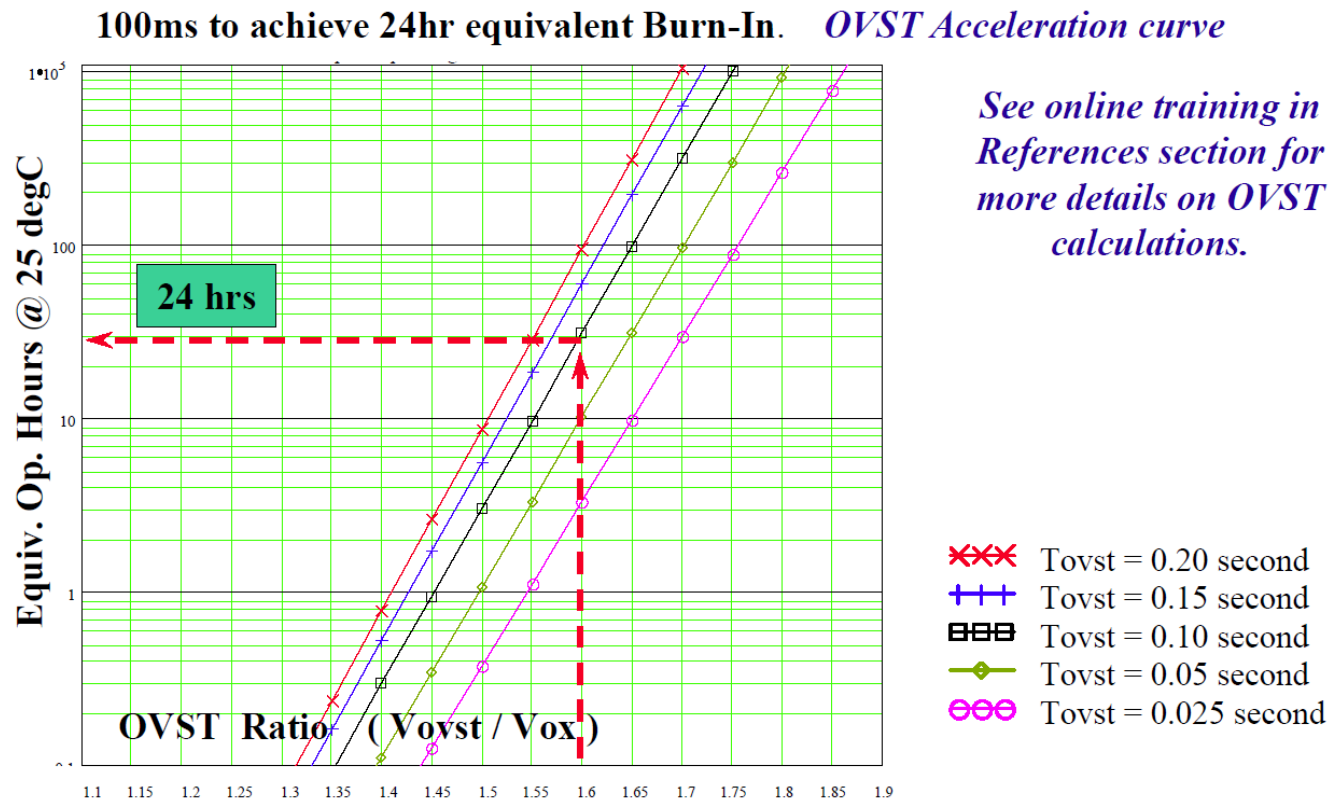
- OVST
- IDDQ
- BVDSS
- SOA

OVST

- **OVST –Over Voltage Stress Test**
- **Need for OVST**
 - Reduce DPPM & customer returns due to random fabdefects
 - Avoid need for burn-in, due to upstream detection of defects
 - Shorter loop from probe test to fab if defects increase dramatically
- OVST -voltage stress test that accelerates Oxide defect failures
- OVST required on any device that has oxide area $> 10K \mu m^2$
- Provides equivalent of burn in with out its costs & problems
 - TARGET : 24 Hrs (25° C Burn-in @Vop,max)
- OVST test sequence
 - 1.Measure current before stress (nom or max operating voltage)
 - 2.Apply OVST stress voltage (measure current during stress for info only)
 - 3.Measure current after stress (same condition as step 1)
 - 4.Calculate Delta current before and after stress. Need to be practically zero

OVST -Continued

- Trade off between ratio of OVST stress voltage & test duration =device voltage max rating to test time
- Recommended OVST stress voltage = 1.6X Max operating voltagefor 100mS to achieve 24 hr equivalent burn-in

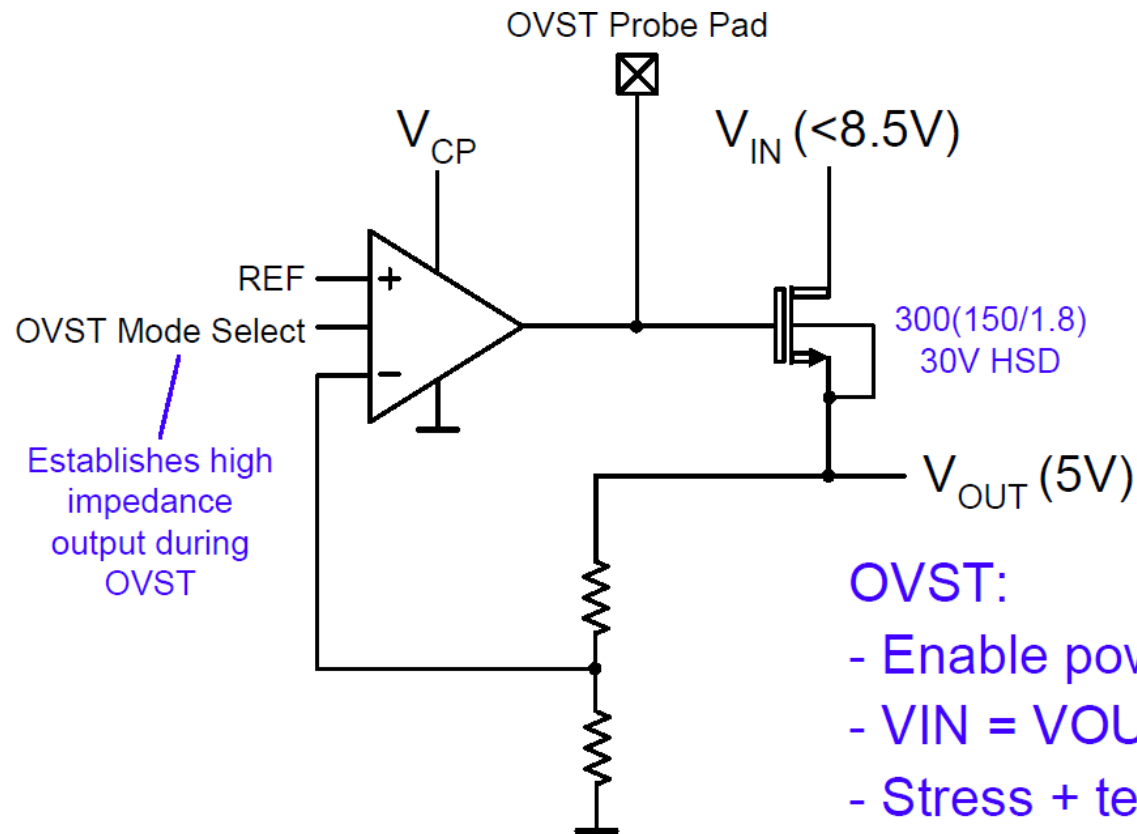


OVST -Continued

- Circuits need to be in sleep state (Current draw should be very small μ A) and components should be able to withstand OVST voltage
- Design for OVST testing is challenging
 - Direct method (across DUT) or indirect method (DUT through other devices) can be implemented
 - Additional probe pads or OVST test bus may be needed
 - A bond out option may also be required
- Group devices with similar voltage ratings. Stress as many of these groups in parallel to save test time
- Typical gate oxide short is in the order of few hundred Ohms. Expect nA to mA of leakage current after OVST breakdown
- OVST implemented in parallel with other tests like digital IDDQ, logic scan, current limit tests etc.
- OVST current should be simulated during top level design verification by adding a few hundred Ohms across the gate oxide

OVST Example

Example of direct method of OVST testing



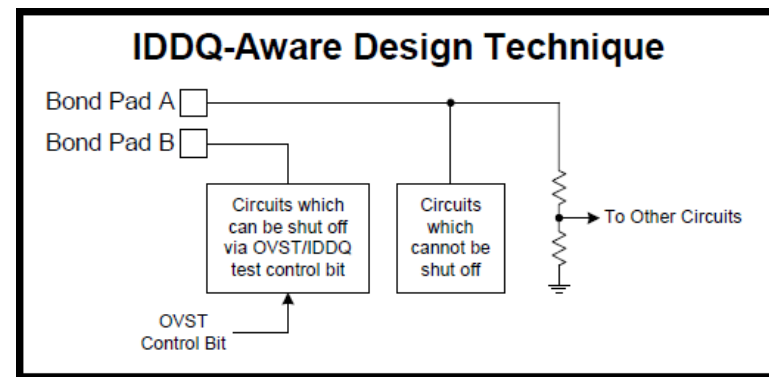
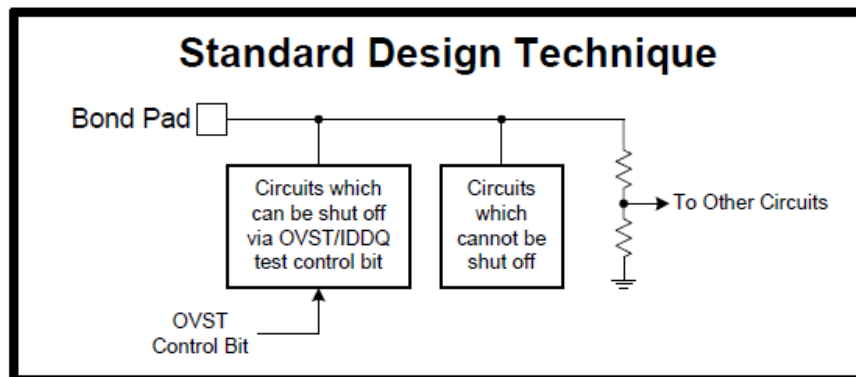
- OVST:
- Enable power-down
 - $V_{IN} = V_{OUT} = 0V$
 - Stress + test at pad

What is *IDDQ*?

- **IDDQ**= QUIESCENT SUPPLY CURRENT (in lowest power mode)
 - Desire lowest current possible to detect small changes due to defects
- **IDDQ DRIFT**= CHANGE IN **IDDQ** POST-STRESS
 - ACCELERATED BY VOLTAGE STRESS
 - TYPICAL LIMITS = FEW 100 μ A
- **Purpose** :
 - IDENTIFY PARTS (or WAFERS or LOTS) with ‘SMALL’ DEFECTS THAT AFFECT SUPPLY CURRENT
 - LEAKY JUNCTIONS
 - ANTENNA DEFECTS
 - SHORTED FETs
 - GOI (Gate Oxide Integrity)

What is *IDDQ*?-Continue

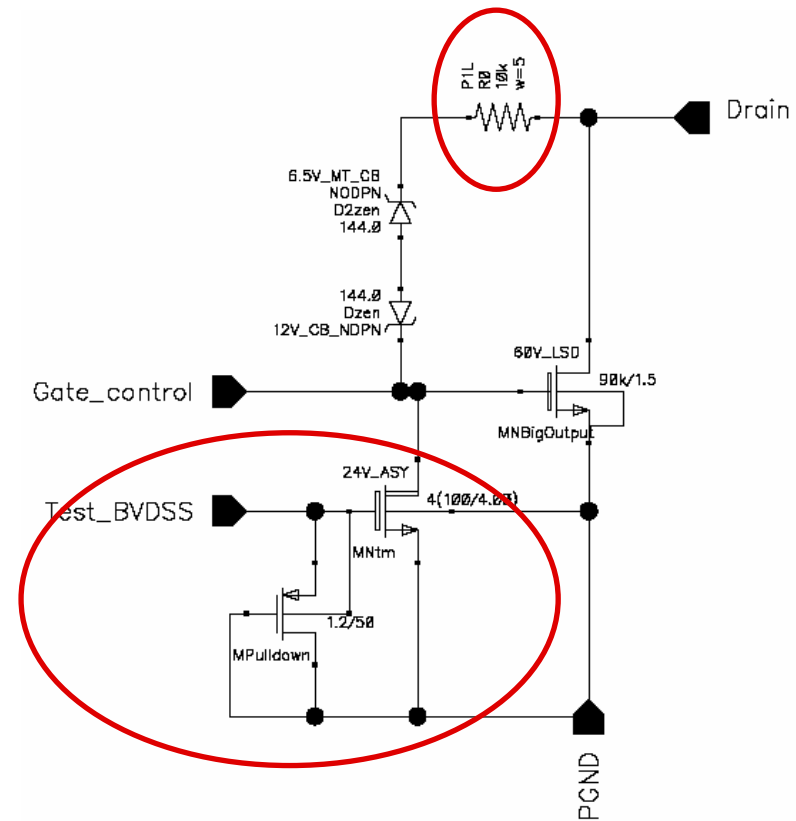
- During OVST stress, pre-and post-IDDQ current is measured at the same pad (“other circuits” must be able to be shut off for IDDQ measurement).
- In Standard Technique, all circuits powered by a supply come from a single source. IDDQ measurements are obscured by circuits which cannot be shut off. (“OVST Control bit” shuts off all current draw in block when high).
- An IDDQ-aware design splits the circuit to two bond pads. Bond Pad B is used for primary IDDQ info, and Pads A & B are joined by bond-out to the package (this technique assumes all OVST/IDDQ testing occurs at probe).



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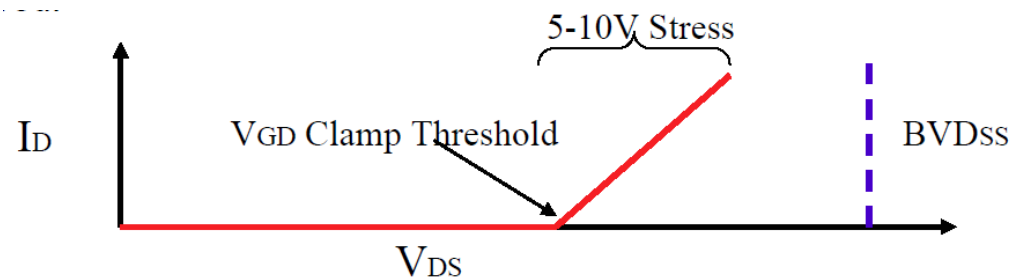
BVdss Test

- BVdss—Breakdown Voltage of Drain with Gate grounded
 - The BVdss test is used to verify that the D-G clamp threshold voltage is sufficiently lower than that of the drain-source breakdown voltage of the device.
- Large FET drivers used for driving inductive loads use a D-G clamp to absorb large voltage spikes by turning ON the FET
- D-G clamp works when voltage is large enough to breakdown the clamp device, pulling up the gate to turn ON the device. The energy is dissipated by shunting the current to supply or ground



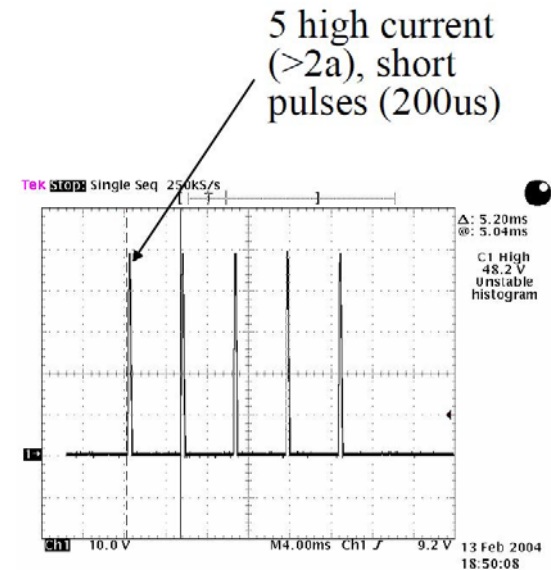
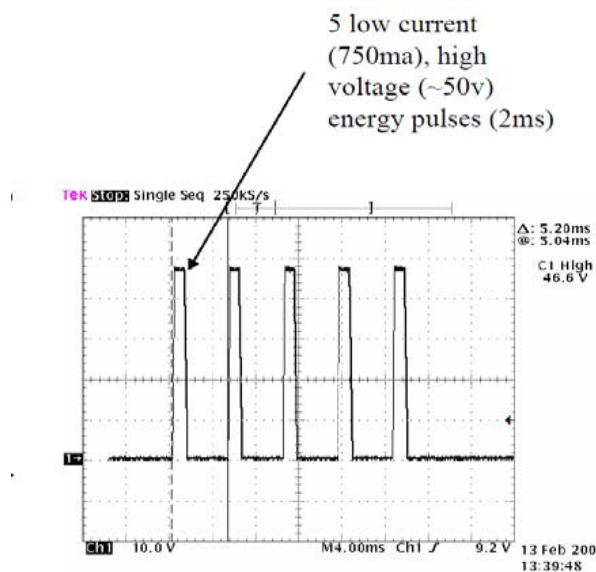
BVdss Test -Continued

- Why BVdss is needed...
 - If the D-S BV is lower and near the D-G clamp breakdown, the energy of voltage spikes may be dissipated by breaking down the device rather than turning it ON with the clamp. This is far more stressful to the device.
 - This test accelerates the defect failure by applying greater than nominal voltage to D-G connection
- A test mode is added to keep the large device turned OFF by shorting G-S voltage
- Stress D-S beyond max clamp voltage but less than min device breakdown value (from PCD)
- A current limiting resistor is added in the clamp path, test leakage currents before and after BVdss test to verify no damage has occurred



SOA Stress Test

- SOA –**S**afe **O**perating **A**rea
- SOA test stresses large FET drivers by emulating max allowable energy to be dissipated by inductive fly back.
- Weak devices can pass R_{dson} and I limit tests. So, devices are forced to dissipate energy levels resembling that of the max allowed in system
- Verify using low level leakage tests that nothing has changed before and after these tests.



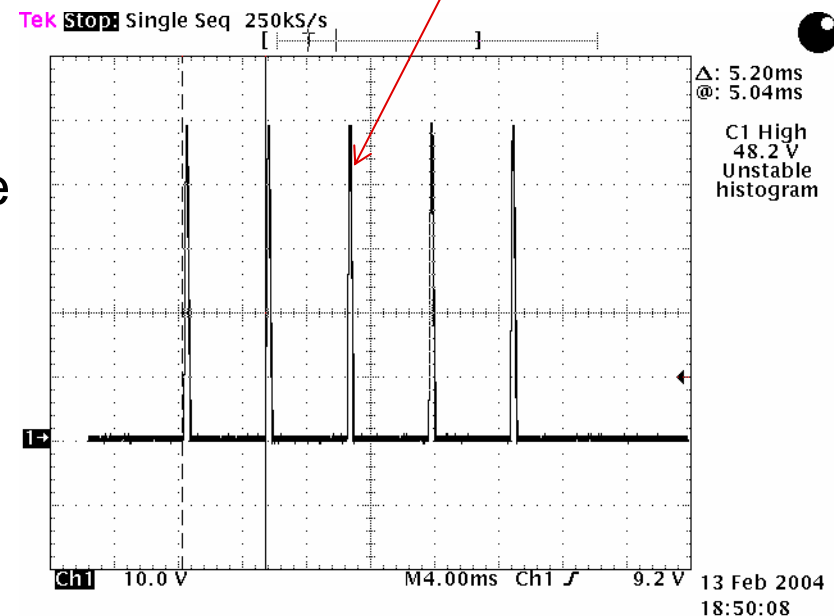
SOA Stress Test -Continued

- The test is performed by subjecting the output to two different stresses. Each stress consists of a pulse-train of 5 current pulses. The pulse width and current value are varied between the two pulse-trains.
- This purpose of this test is to stress the device to the maximum extent it may encounter in the customer's system. This can be dangerous as the potential for creating walking wounded parts is quite high. Much care should be taken when determining values and planning for test robustness.
- The SOA testing is begun by performing a low-level leakage measurement on the device. Pre and post stress leakage measurements will be compared to verify that no damage has occurred to the device. This is critical and must be evaluated carefully. Most likely, failures of this test will show leakage variation between pre and post measurements, but may still be functional and pass other parametric tests.

SOA Stress Test -Continued

- Stress 1(High Current Pulses): This test is performed by setting the current to the maximum current expected from the fly back of the inductive load. This is typically specified as the maximum allowable current through the device. The pulse width is set to 200uS (200uS chosen because it is the fastest most ATE instruments can accurately generate such a pulse).
- High current pulse train validates the max current handling / power handling capability of the LDMOS.

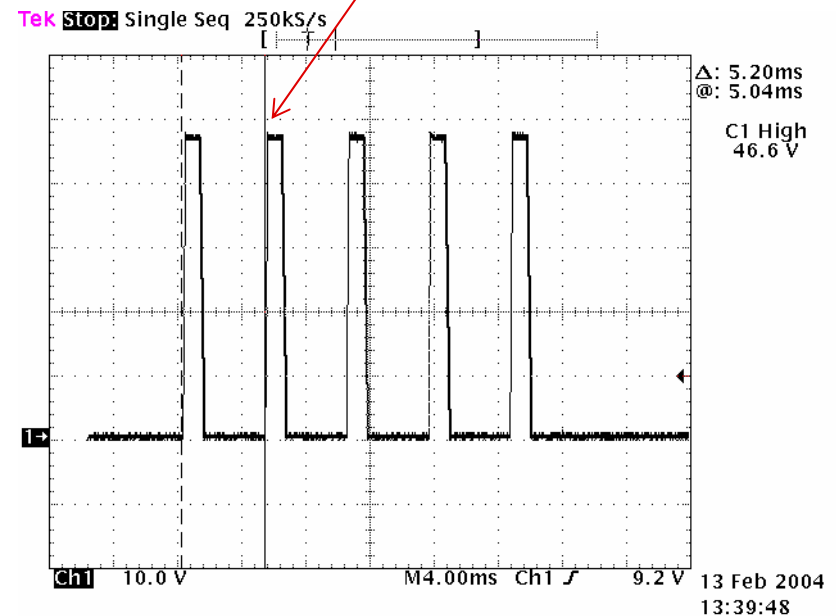
5 high current (>2a), short pulses (200us)



SOA Stress Test -Continued

- Stress 2 (Low Current Pulses): This test is performed by setting the current, pulse width, and duty cycle to replicate the maximum amount of energy required to be dissipated by the device.
- Low current pulse validates the energy handling capability of the LDMOS.
- Compare the low-level leakage measurements made before and after the SOA stresses to **verify nothing has changed in the device.**

5 low current (750ma),
high voltage (~50v)
energy pulses (2ms)



What is 'AEC Q100'?

- Defined by the Automotive Electronics Council (AEC)
- Original AEC members were: Chrysler, Delco Electronics (GM), and Ford
- The published base specification for Semiconductors is: AEC Q100
- The first version of AEC Q100 was published in 1994

- AEC Q100, and the supporting documents, sets standards for :
 - Qualification Requirements and Methods
 - Production Testing
 - Documentation
- <http://www.aecouncil.com/>

What are the AEC Q100 documents?

- **AEC - Q100 Rev - G base:** Stress Qualification For Integrated Circuits (base document only with no test methods)
 - **AEC - Q100-001 - Rev-C:** Wire Bond Shear Test
 - **AEC - Q100-002 - Rev-E:** Human Body Model (HBM) Electrostatic Discharge Test
 - **AEC - Q100-003 - Rev-E:** Machine Model (MM) Electrostatic Discharge Test
 - **AEC - Q100-004 - Rev-D:** IC Latch-Up Test
 - **AEC - Q100-005 - Rev-D1:** Non-Volatile Memory Program/Erase Endurance, Data Retention, and Operational Life Test
 - **AEC - Q100-006 - Rev-D:** Electro-Thermally Induced Parasitic Gate Leakage Test (GL)
 - **AEC - Q100-007 - Rev-B:** Fault Simulation and Test Grading
 - **AEC - Q100-008 - Rev-A:** Early Life Failure Rate (ELFR)
 - **AEC - Q100-009 - Rev-B:** Electrical Distribution Assessment
 - **AEC - Q100-010 - Rev-A:** Solder Ball Shear Test
 - **AEC - Q100-011 - Rev-C1:** Charged Device Model (CDM) Electrostatic Discharge Test
- . Not all tests apply to all devices

What are the AEC Q100 Grades?

There are 5 grades, based on the AMBIENT operating temperature.

Grade 0: -40° C to $+150^{\circ}\text{ C}$ ambient operating temperature range

Grade 1: -40° C to $+125^{\circ}\text{ C}$ ambient operating temperature range

Grade 2: -40° C to $+105^{\circ}\text{ C}$ ambient operating temperature range

Grade 3: -40° C to $+85^{\circ}\text{ C}$ ambient operating temperature range

Grade 4: 0° C to $+70^{\circ}\text{ C}$ ambient operating temperature range

Grade 1 is the most common, followed by Grade 2

(1) Above PSRR region is referred from TI literature number sylt202, "Understanding power supply ripple rejection in linear regulators".

What is NOT part of AEC Q100?

- AEC Q100 does NOT require testing for 'Immunity to Conducted Transients' for devices that are connected directly to the battery
 - SAE-J1113
 - ISO-7637
- There are 8 different Conducted Immunity Test Pulses, two most common are:
 - Load Dump (Test Pulse 5A)
 - Starter Motor Engagement, aka 'Cold Crank' (Test Pulse 4)
- AEC Q100 does NOT require Reverse Battery (V_{IN} below GND), Reverse Bias ($V_{OUT} > V_{IN}$), Reverse Leakage (V_{OUT} to V_{IN}), V_{OUT} Shorted to Battery (or V_{IN}), or other Fault conditions be ensured.
 - However, individual Automotive customers could ask for characterization information for these conditions on a case-by-case basis, or they could insist that the conditions be added to the datasheet and ATE tested.