高速数字信号眼图测试优化

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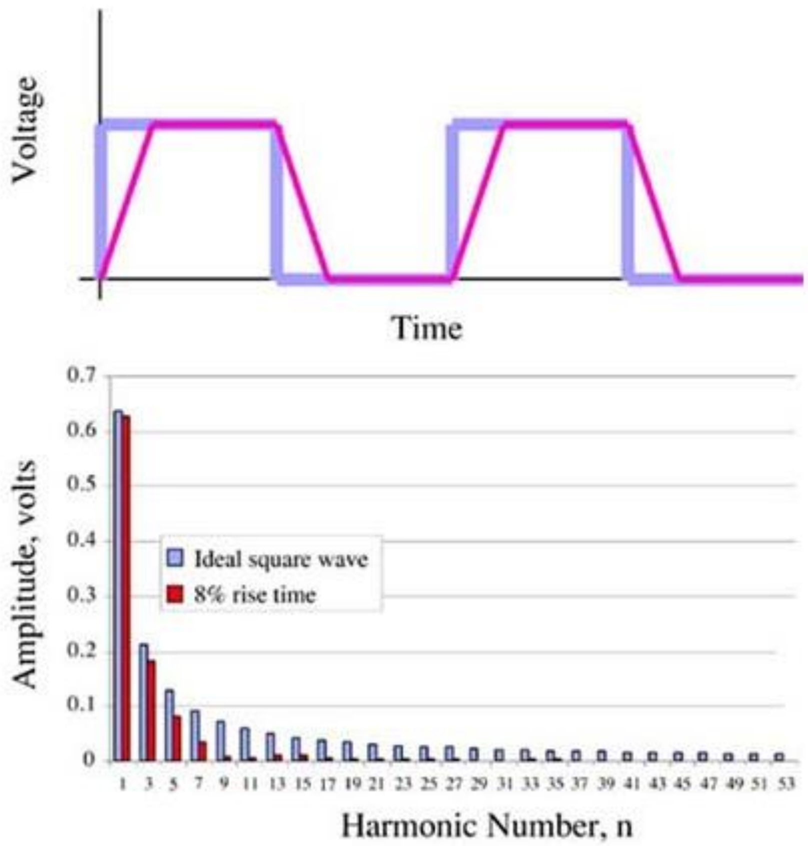
Contents

- High Speed digital concept
- High Speed digital common test items
- Jitter and Eye tests
- Eye test with equivalent sampling

High speed digital test challenge

- Digital signal is a combination of 0,1;
- Compared with analog/RF signal, it actually required higher bandwidth;
- The higher data rate require higher bandwidth of tester hardware;



Industry's High Speed Interfaces

- DDR (4/5)
- USB 3.x
- DVI/HDMI (2.x)
- S-ATA (3.x)
- PCI-Express(3/4)
- DisplayPort
- MIPI
- RDRAM
- IEE1394
- HyperTransport I
- Rapid IO (RIO)
- XDR (Yellowstone)
- Flex-IO (Redwood)
- XAUI
- FB-DIMM/AMB

Typical speed

	application	Type	datarate_per_lane
HDMI	Multi-media, video+audio	HDMI2.0	6Gbps
		HDMI1.4	3.4Gbps
USB	mass strorage;	USB3.0	5Gbps;
		USB2.0	480Mbps
SATA	Mass strorage; Interconnection for PC	SATA3.0	6Gbps
		SATA2.0	3Gbps
PCIE	PC extension; workstation;	PCIe 3.0	8Gbps
		PCIe 2.0	5Gbps
DDR	Memory	DDR4-3200	3.2Gbps per pin
		DDR4-2400	2.4Gbps per pin

High Speed common test items

- Receiver
  - at speed functional
  - impedance
  - sensitivity
  - jitter tolerance
  - rx skew
  - setup/hold time
  - …

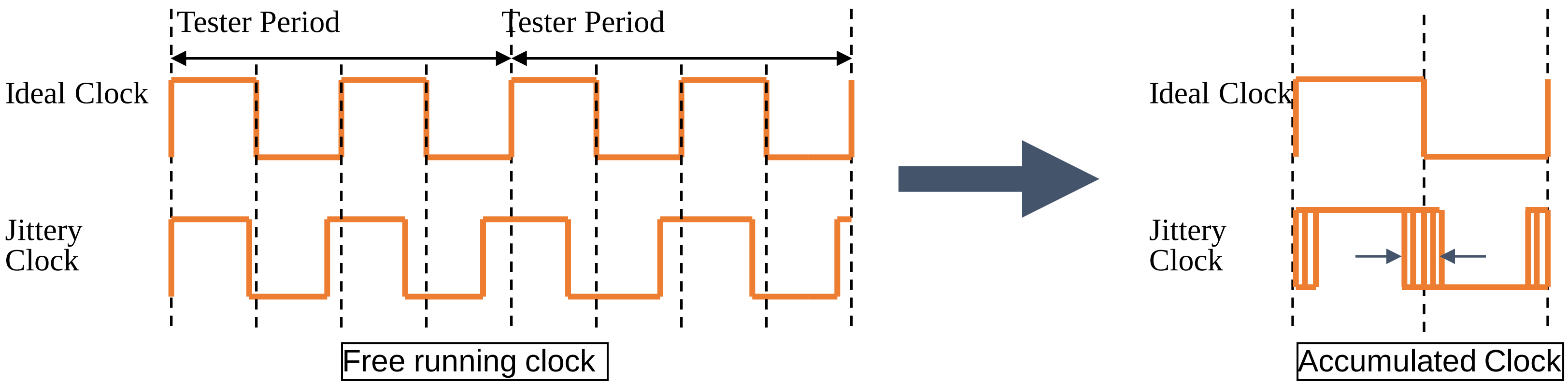
High Speed common test items

- Transmitter
  - at speed functional
  - impedance
  - skew
  - pll freq
  - jitter
  - BERT
  - histogram
  - swing
  - rise/fall time
  - eye test/fast eye mask
  - …
- Loopback

Jitter and Eye tests

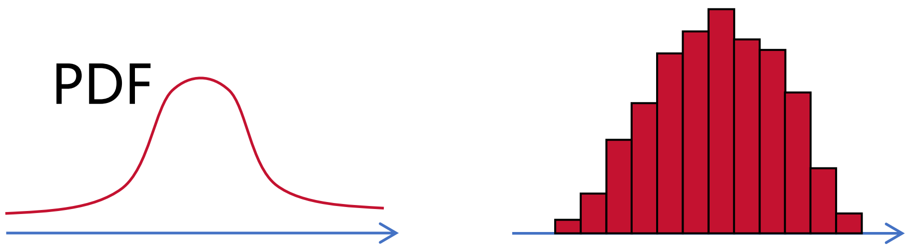
Definition of Jitter

- Jitter – Unwanted variations on a signal such as the interval between successive pulses, the amplitude of successive cycles, or the frequency/phase of successive cycles.



Jitter Histogram

- Histogram is a statistic method to illustrate distribution of targeted parameter. Height of each bar is proportional to possibility value h this bin.



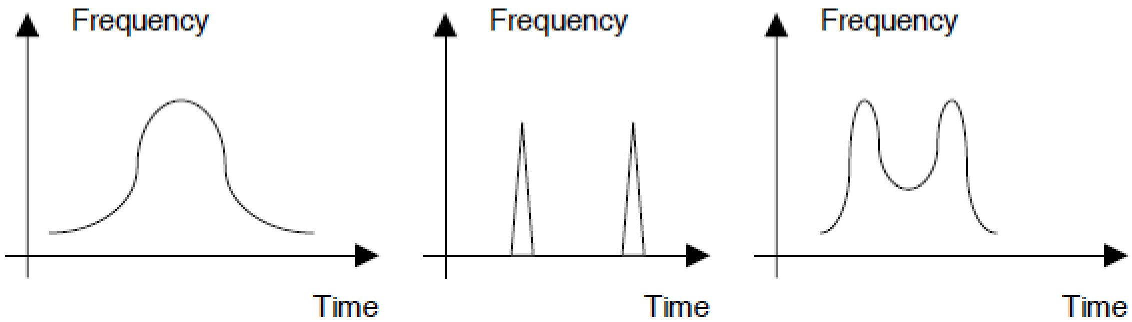
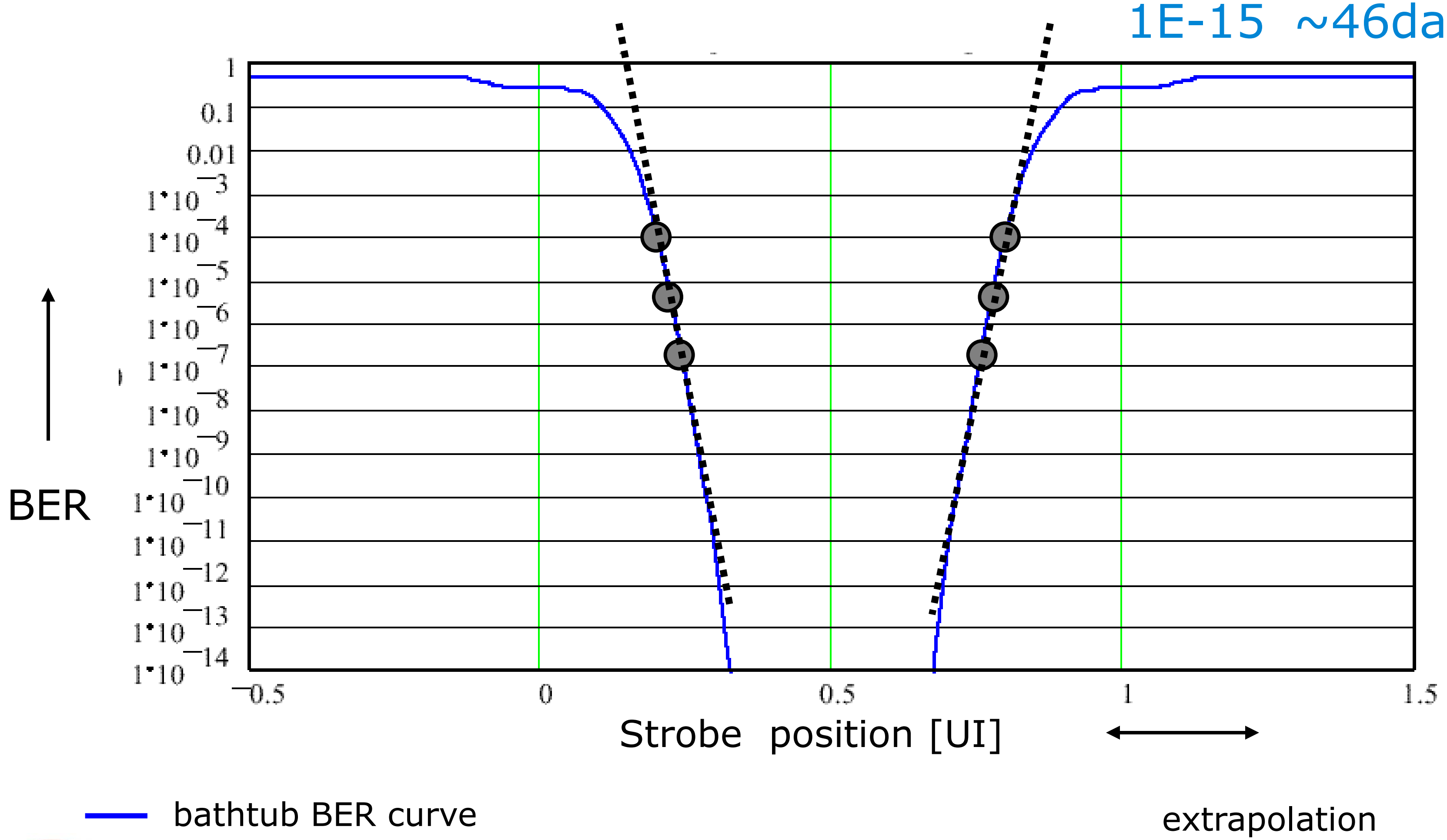


Fig. 9: Histograms of random Jitter, deterministic jitter, combined DJ & RJ jitter

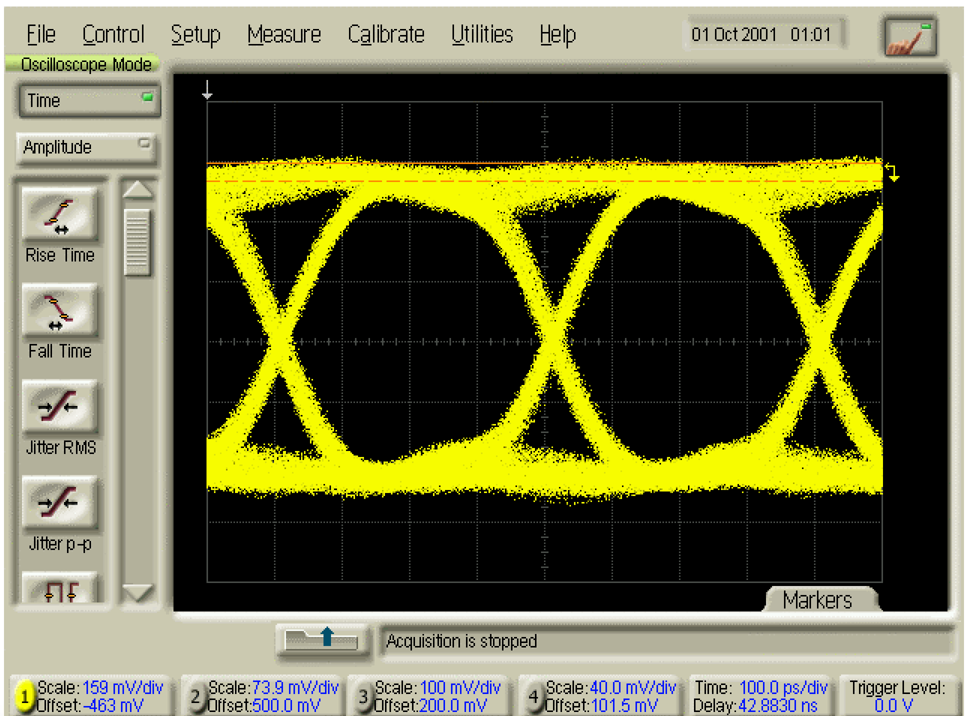
BER Solution: Extrapolation

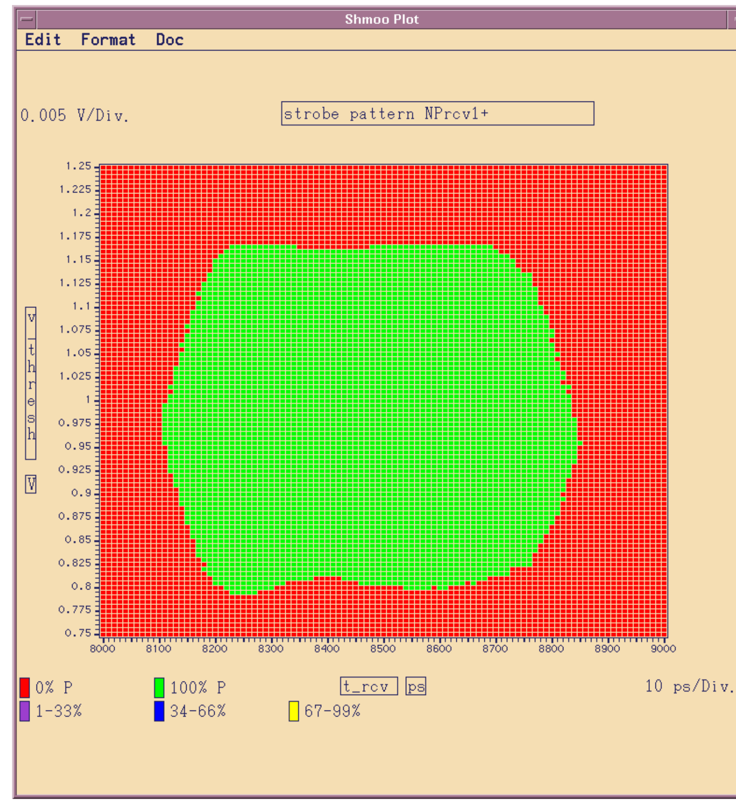
Data Rate=2.5Gbps
1E-4 ~40μsec
1E-12 ~1hour
1E-15 ~46days



Definition of an "Eye Diagram":

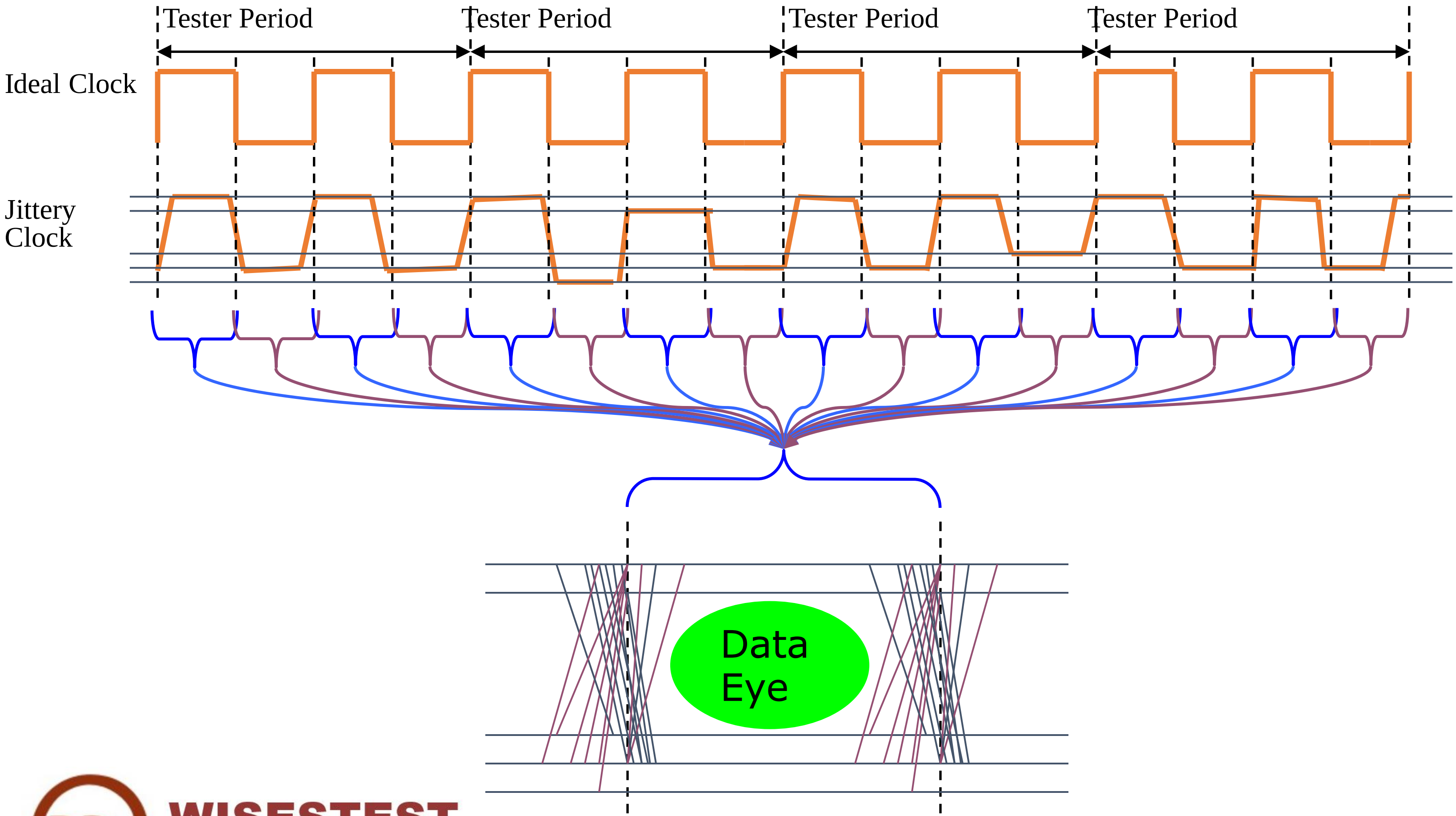
- Definition: Superposition of many data waveforms acquired from some test instrument (sampling oscilloscope or 93k) based on a constant trigger
- Eye Diagrams are commonly used to characterize high speed interfaces





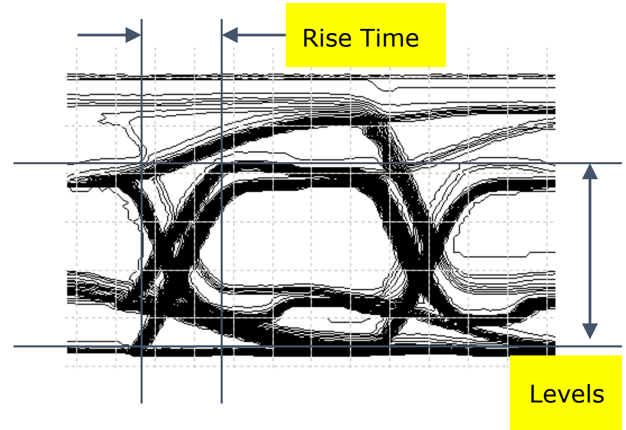
How is an Eye Diagram Derived?

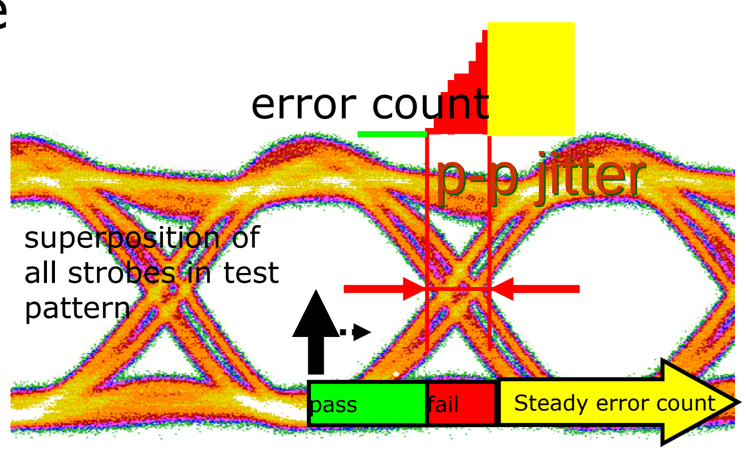
Example: Clock signal from the device

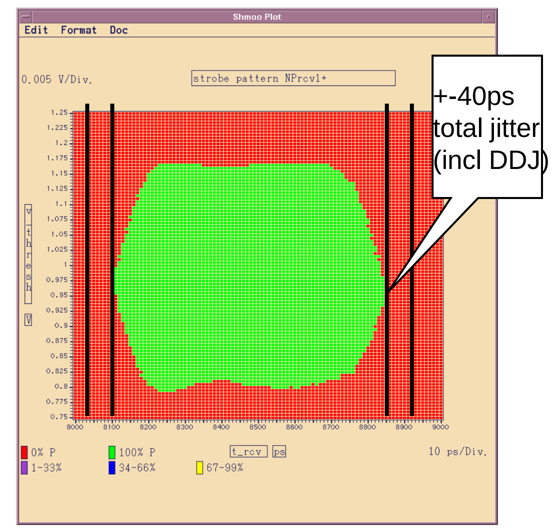


What information in Eye Diagram?

- Eye Width
- Jitter
- Rise and Fall Times
- Signal Levels
- Overshoot and Undershoot
- Ripple

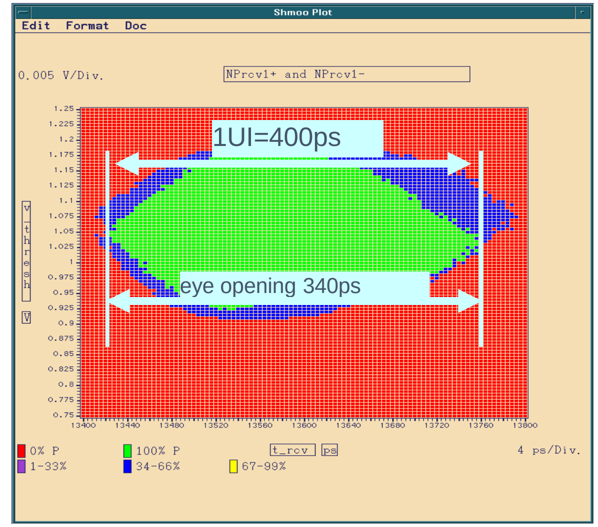


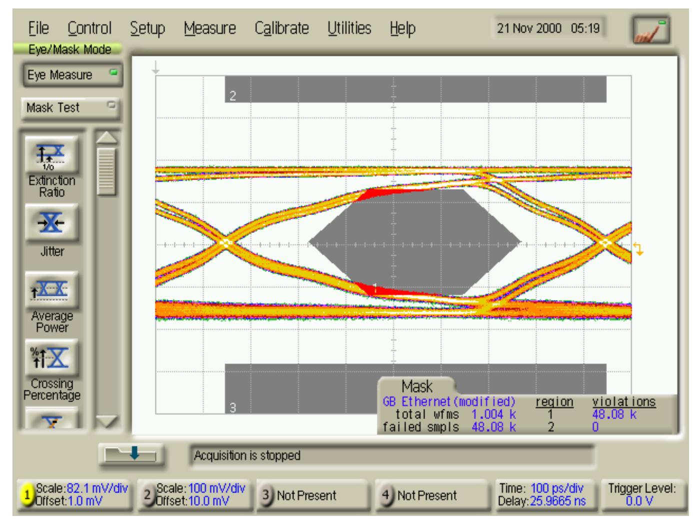




Eye test: shmoo

- Functional pattern based eye test: strobe each bit;
- X: search strobe edge;
- Y; search threshold voltage;
- Each X&Y combination, run pattern. Get pass/fail, draw shmoo.





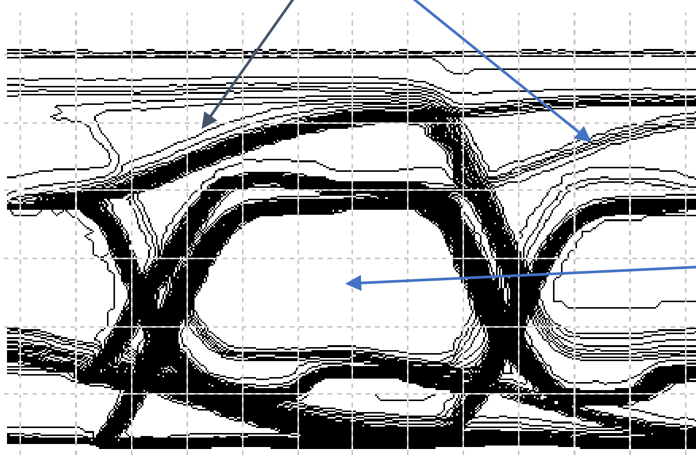
Eye test with equivalent sampling

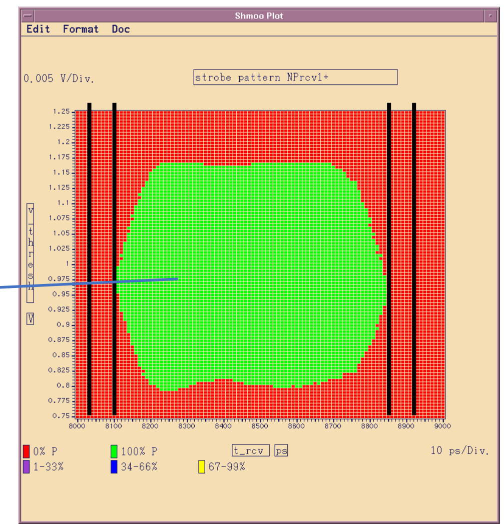
- Improved eye measurement solution

Motivation

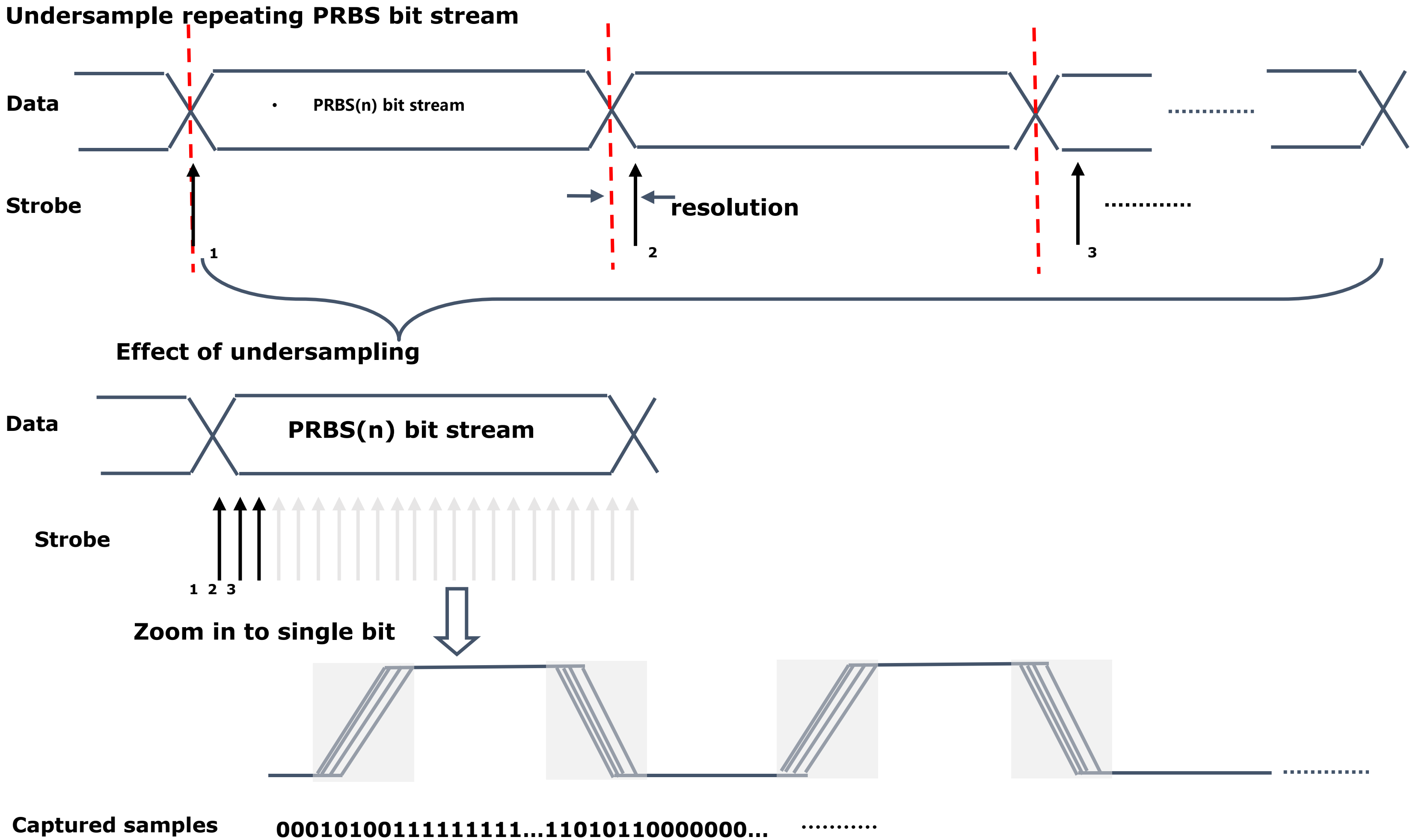
- Traditional eye diagram measurement only show passing area, information in "failed" region is missing.

Missing information

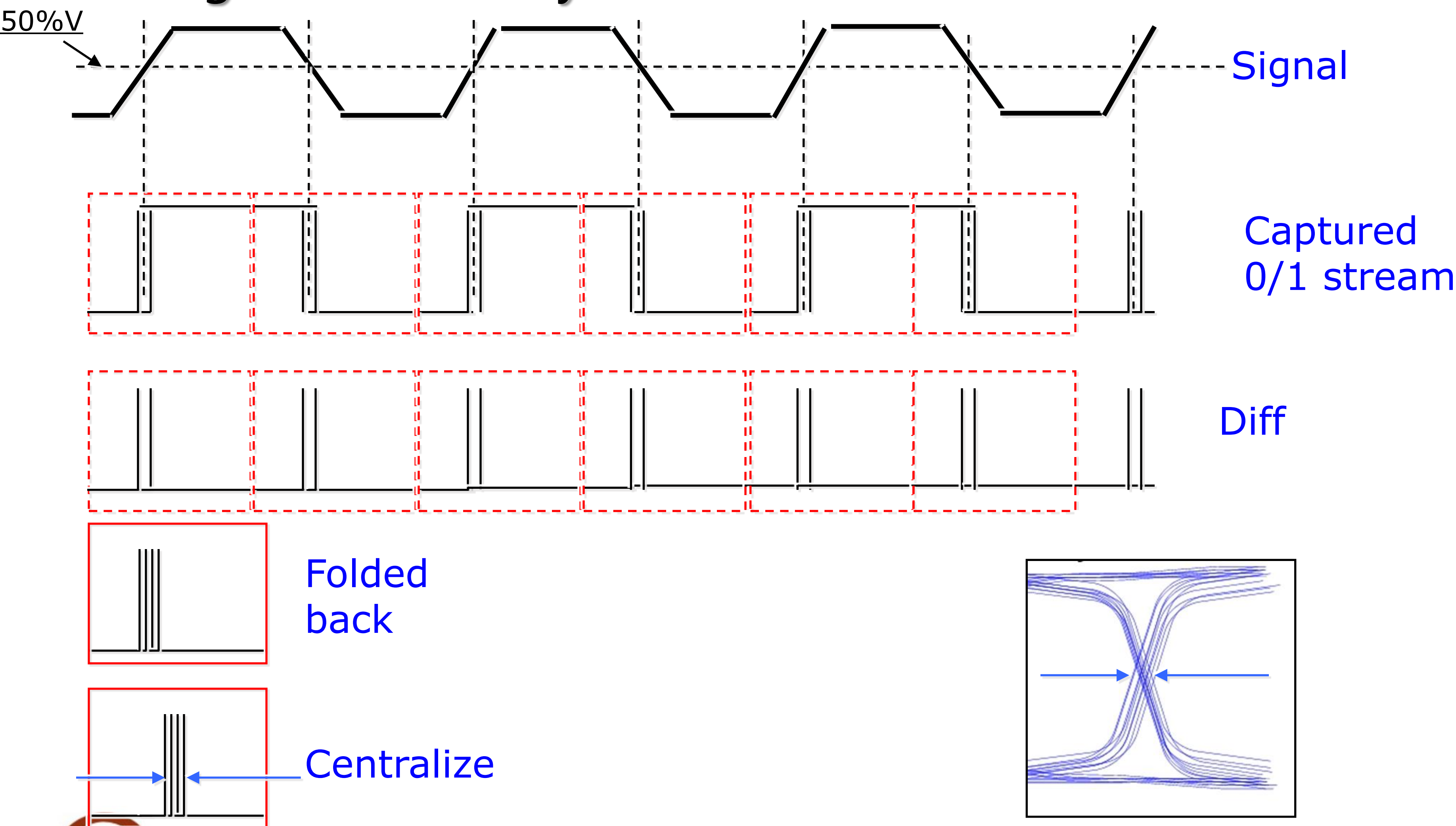




Eye Test with walking strobe Solution

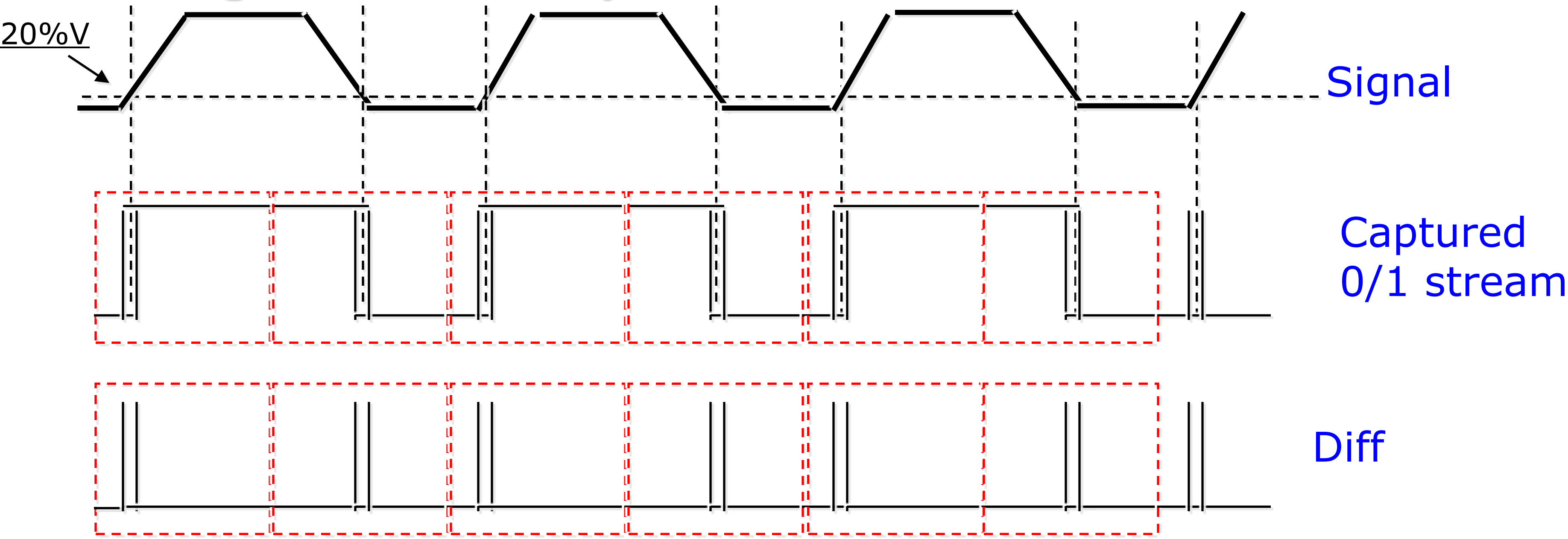


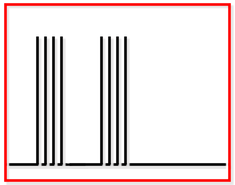
Eye Test Solution
- Algorithm: 50% Eye



Eye Test Solution

- Algorithm: 20% Eye





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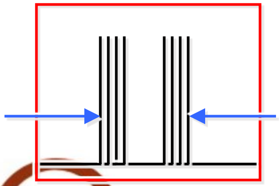
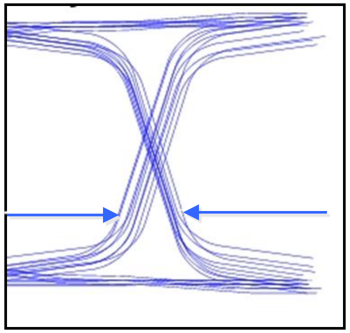
back

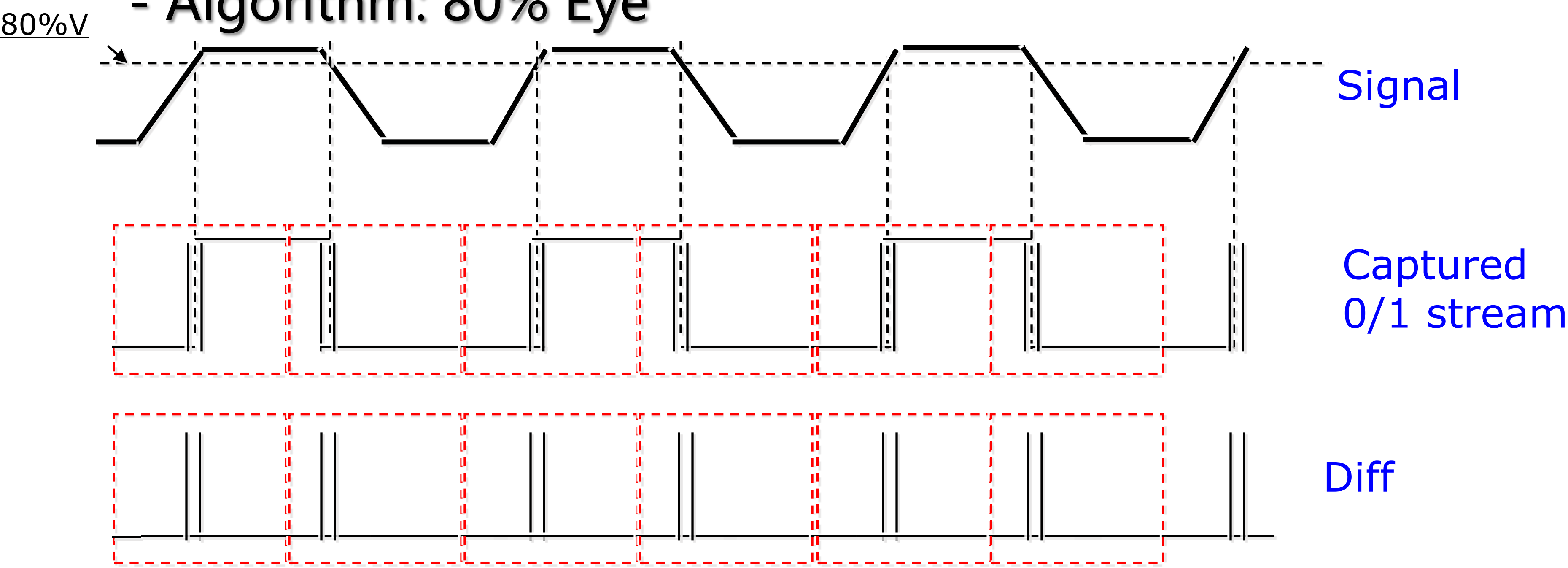


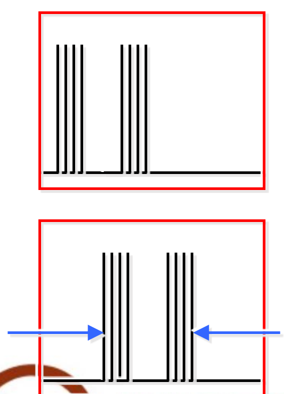
Centralize
Based on eye50

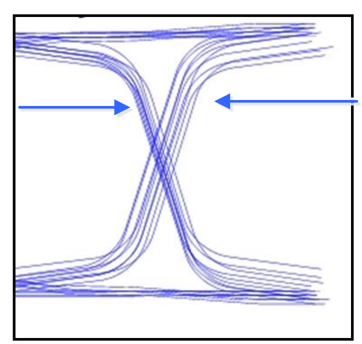


Eye Test Solution

- Algorithm: 80% Eye

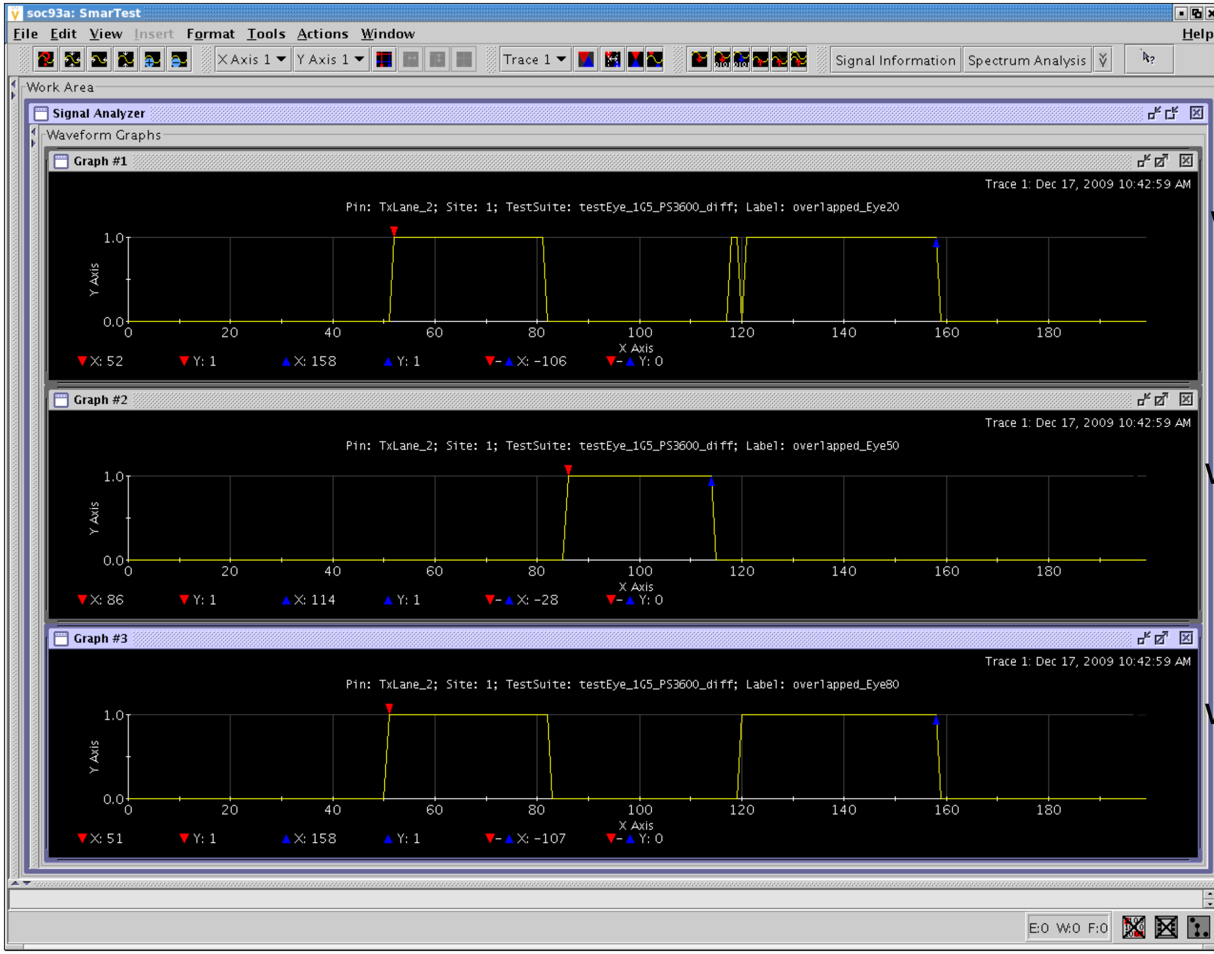






Based on eye50

Eye Test Solution

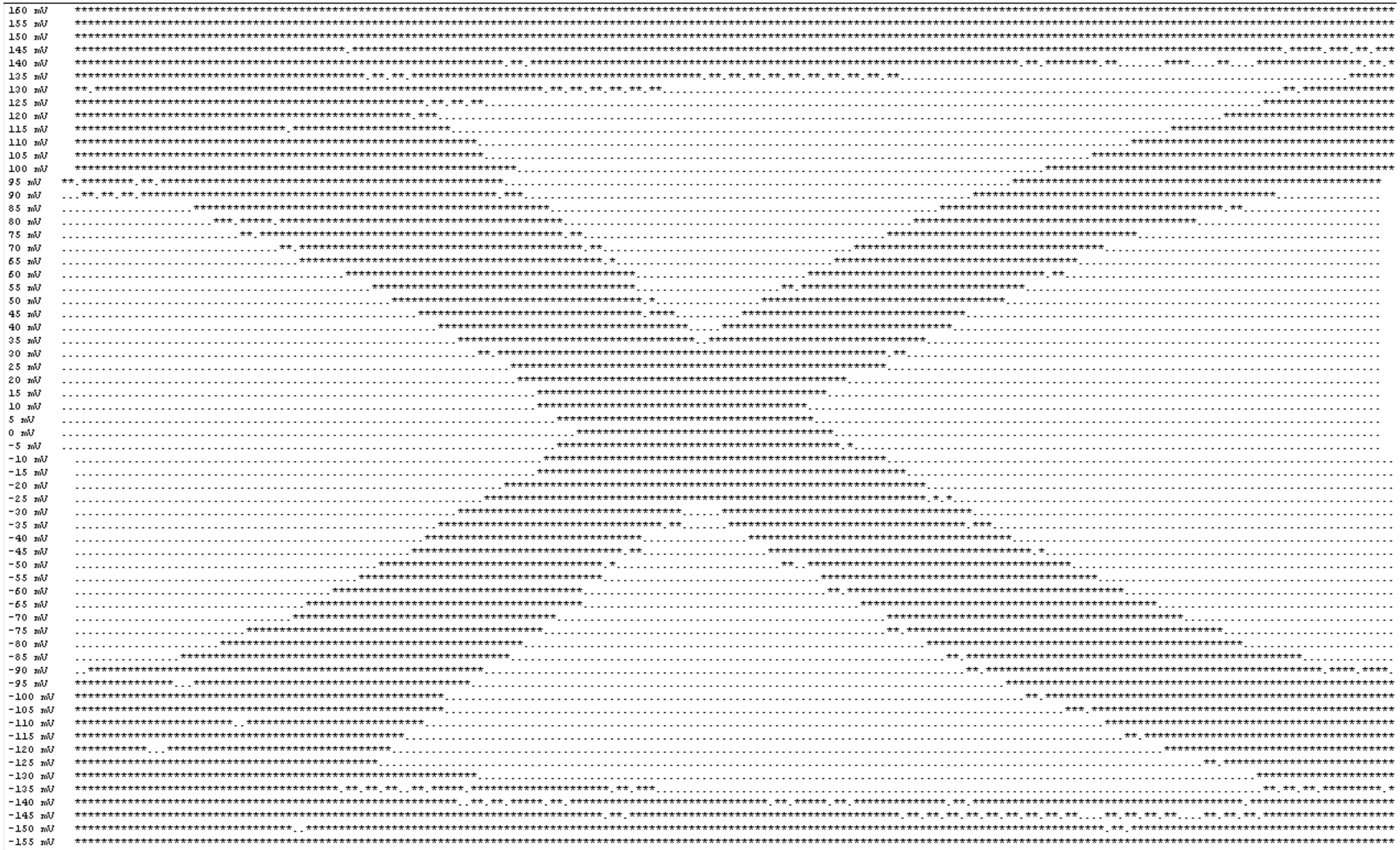


width(20% eye) ~ 0.45 UI

width(50% eye) ~ 0.85 UI

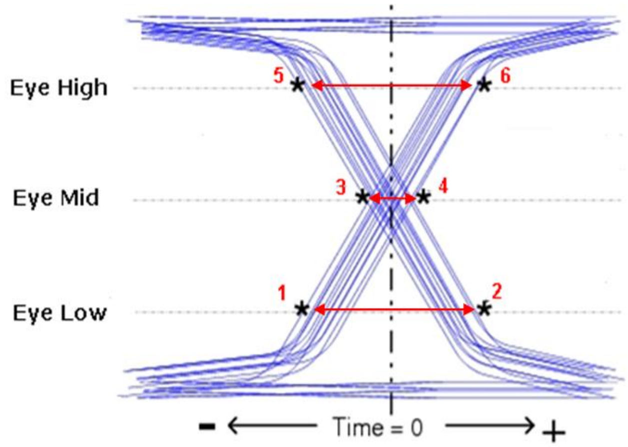
width(80% eye) ~ 0.45 UI

Eye Test Solution Results



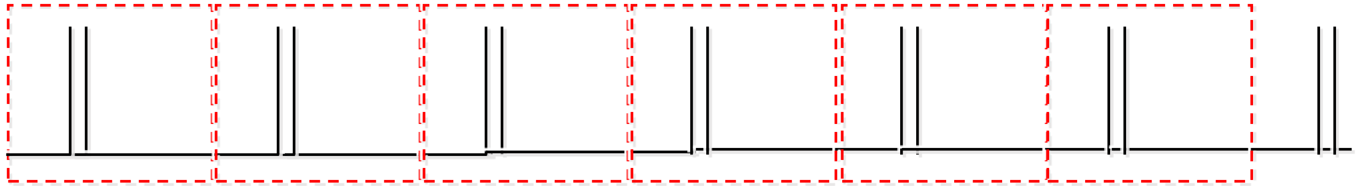
Usage in Production test

- How to use in production test?
  - Reduce level search steps, saying 3 level: 20%, 50%, 80%; calculate rise time, fall time, jitter;
  - Use hidden upload feature;

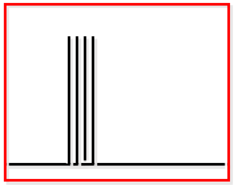


Histogram

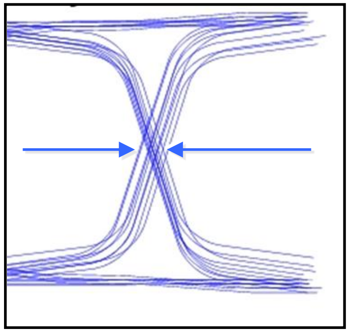
- Can we get histogram?

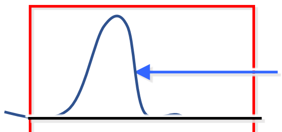


Diff

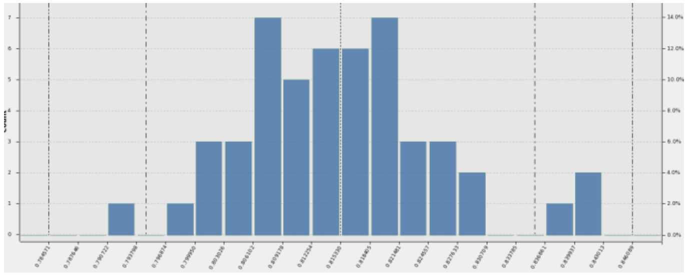


Folded back, replace
OR with ADD



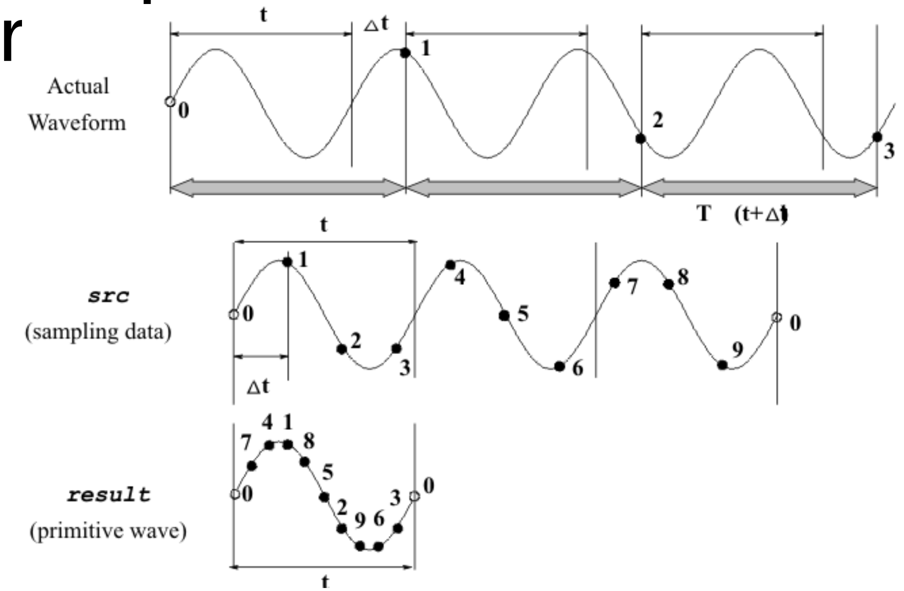


Histogram



Undersampling and shuffle

- Walking strobe is a extreme example of undersampling.
- Consider replace below sine wave with PRBS str



- If tester has higher sampling rate, we can increase sample rate, to reduce pattern time.

Timing design example I

● Test condition

SATA II Data rate=3.0Gbps

UI=1000/3.0=333.333ps

PRBS7 input data stream (127bits)

Resolution=1UI/200=1.667ps

=>

◆Method1: walking strobe

sample period=UI*127bits+resolution=42.335 ns

Sample rate = 23.621Msps

Sample number=127*200=25400;

Timing design example II

● Test condition

DDR5 Data rate=4.0Gbps

UI=1000/4G =250ps

Compared pattern (1000 UI)

Resolution=UI/250=1ps

=>

◆Method: coherent sampling and shuffle

Sample number N=1000*250=250000;

Coherent: M/N=ft/fs; fs=ft*N/M=4MHz*250000/M

M=250001, ft= 3.9999840MHz, period=250.001 ns

M=251, ft= 3984.0637450MHz, period=251 ps (PS9G support)

Summary

- Advantages:

Get more information out of pass area;

No need to use high sampling rate, only assure channel bandwidth is enough;

No need to do payload search, to find exact start point;

Data process is simplified by using "diff", no need to compare bit by bit.

- Disadvantages:

Pattern is repeatable;

Tester supports multi clock domain;

附录

- 公司简介：

　　巍测科技专注于芯片测试方案开发，利用丰富的业界经验，为客户提供优质的测试服务；创始人团队都有超过10年的从业经验，对高速数字信号测试和RF SOC测试有丰富经验，熟悉A93K等高端测试机台；

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