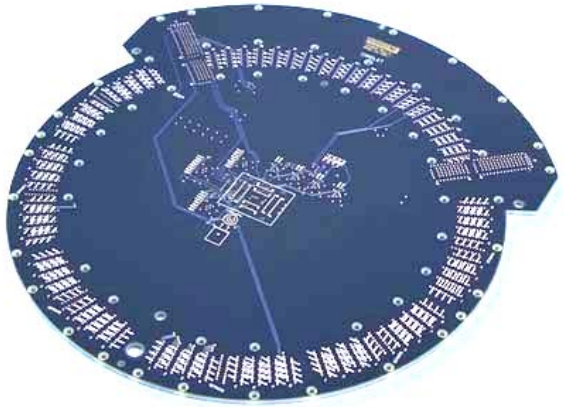
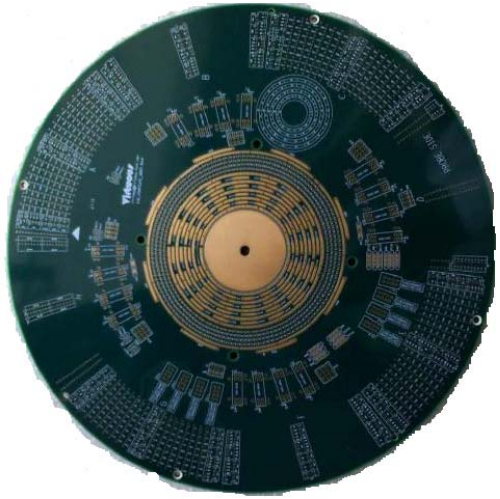
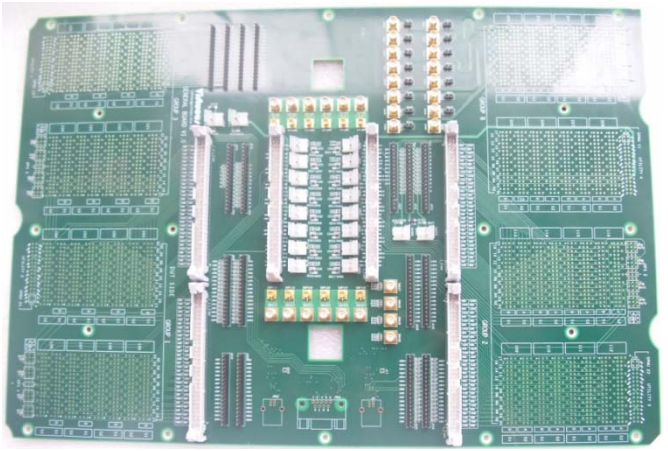
ATE Board Training

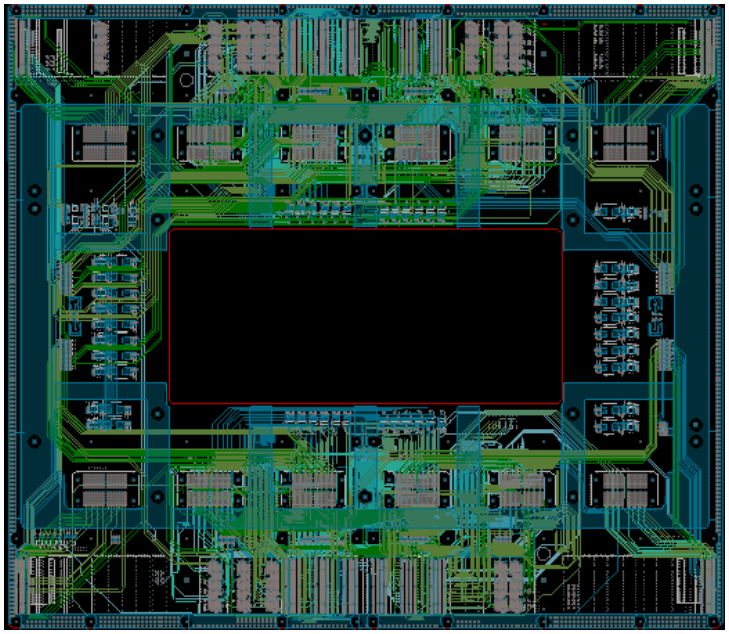
High Speed Load Board and Probe Card PCB Design







High Speed Load Board and Probe Card Design



Part 1 Mechanical Part

Part 2 Electrical Part

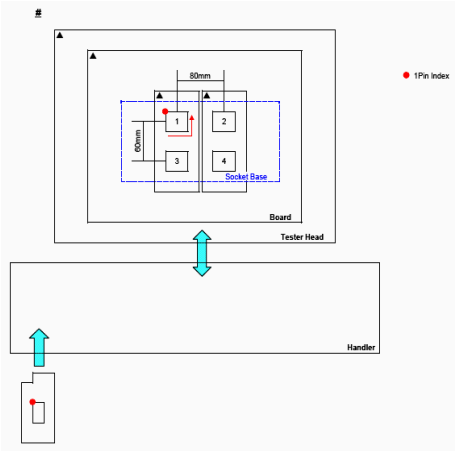
Part 3 PCB material

Part 4 PCB manufacture

Part 1 Mechanical Part

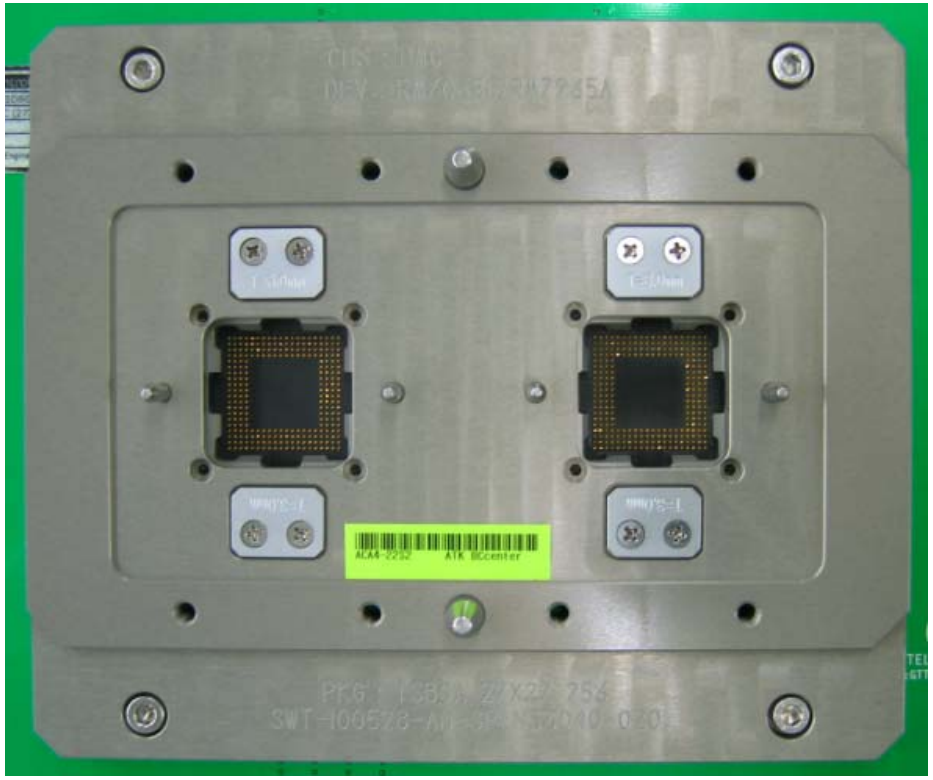
Pay special attention to the important points.

Pin 1 position and orientation



- When mark pin 1 position and orientation of socket pins on it. Please always reference the guide pin holes or if the guide holes are symmetrical, then use the test channels.
- We marked 12 O'clock position for your easy reference. The 12 o'clock position is where the cable of test head is located.
- In other words, the operator stands at 6 o'clock position and faces the test head which is located at 12 o'clock.

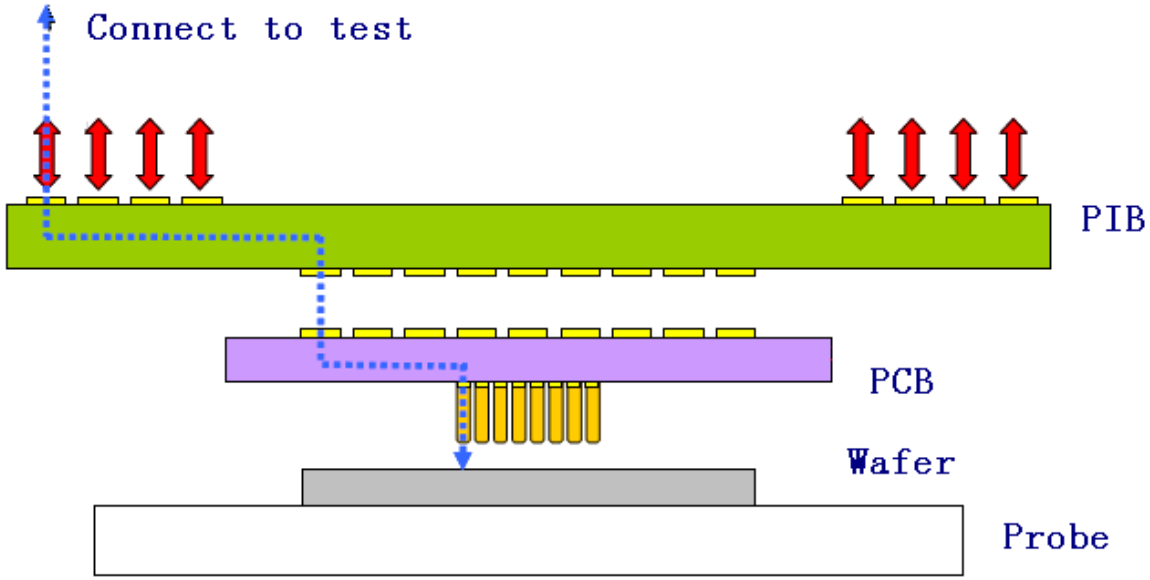
Handler Docking



- This is most confusing and mistakes are often made.
- We may or may not have this information. But we know who makes the contact plate and whether he has the contactor Plate drawing.
- If the contact plate drawing is not available, Always get the handler model and use name. Get also the device tray drawing.

Probe card pin 1 and orientation

- Customer will have to give you the die bond and diagram. Make sure the drawing is for viewing from the prober side or from the tester side.



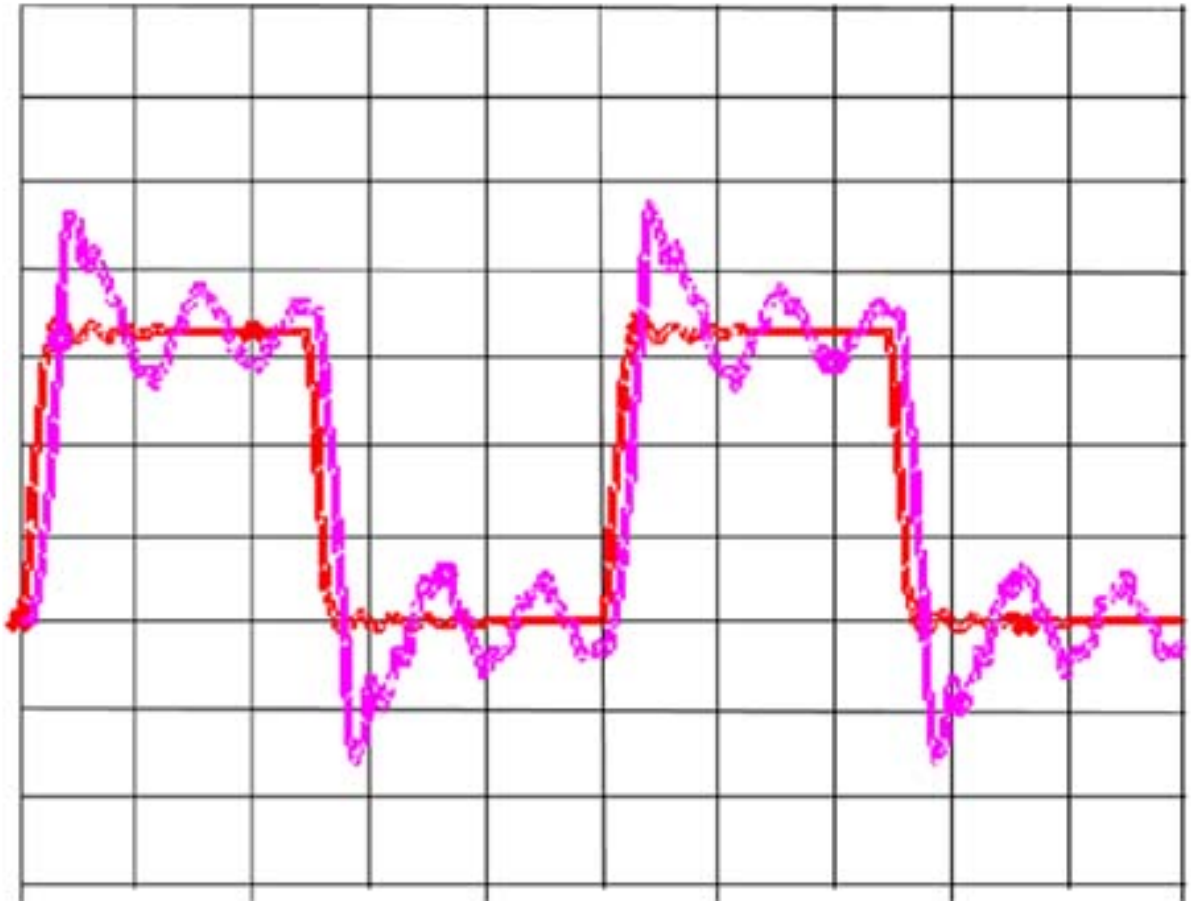
View From

- When we describe the pin 1 and orientation and other features of the board, we refer to viewing from the device side , or handler side, or probe side versus the test side.
- Pl. avoid using top side and bottom side, because when docking with handler, the test head may be rotated upside down , top and bottom side is easy confusing.
- Also please avoid using components side and solder side as components can be put on either side of the board.

Test Config

- We use TC(test channel) population to describe the test channels available on a customer’s test head. This information is important, as we cannot connect traces to channels that does not exist on a customer’s tester.
- Some customers maybe provide test config, We should use the lowest number TC.

Part2 Electical Part



Three Signal

- RF and Microwave

  RF and Microwave circuits tend to have very small amplitude signals at the receiver. So the receiver environment needs to be well protected from noise sources that distort these small signals.

- Analog Signal

  Analog or video circuits convey information in the shape or amplitude of the voltage waveform being sent. As a result it is important to design the circuits over which the signals travel such that distortion and external noise are hold a minimum.

- Digital Signal

  Digital circuits convey information at two different voltage levels, four voltage levels are used. The driver of digital circuits are designed to create signal with voltage levels that are larger than those required by there receivers. As a result, digital circuits can tolerate a significant amount of noise and distortion(loss) and still convey information successfully.

Mixed signal

- For mixed signal design, the ideal way is to separate the digital and analog section on the board. Very often the schematic is not designed in such manner. Please list which analog traces are specially sensitive to noise. We may have to shield those traces by guide line or composite ground.
- For digital traces, we do not recommend using of composite ground.

High speed Signal definition

- Whether is high frequency digital signal decided by signal edge rate. Generally considered signal rise time (Tr) of less than 4 times the transmission time (Tpd), can be considered as the high frequency signal.
- F2=1/ (Tr x π), when F2>100MHz, should be in accordance with the high-frequency signal design.
- The following conditions must according to the high frequency rule design:

  System clock frequency is more than 50MHz

  Rise / fall along a time less than 5ns device

  Analog / digital mixed circuit

Micro stripline and Stripline

- Micro stipline lays on the surface layer of the PCB; it has a faster velocity of propagation than the stripline. This is due to a lower effective dielectric.

  Also, its lower effective dielectric, allows it to have

- Stripline lays sandwiched between two planes.

  The advantages of Stripline are:

  -Very Low Far End CrossTalk

  -Low skin effect(current flow on both surfaces of conductor)

  -No EMI

  -Better protection from hazards

Trace length

- Trace length affects 2 important parameters-capacitance and signal Delay Time.
- In general, the shorter the trace the better.

  For high speed testing trace, capacitance is the most important parameter. High Capacitance on traces will slow down the rising edge. For Critical traces, the lower the capacitance the better. Since capacitance is proportional to the trace length, hence the shorter the trace the better.
- Another direct effect of trace length is signal delay. Most testers have a TDR function, so that the signal delay difference in traces can be skewed within a range. In some cases certain signals must arrive at the test channel within a certain window of time or have equal capacitance, then equal trace length is required.
- Unless this is absolutely, there is no reason to increase the capacitance by having equal trace length.

Delay

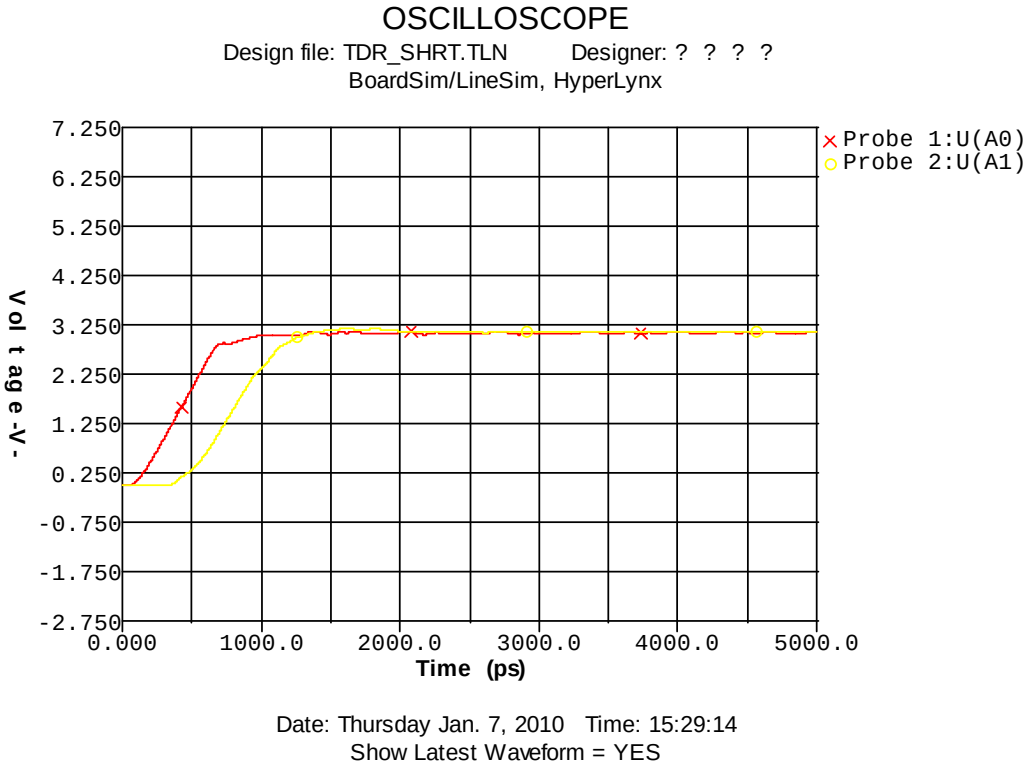
- Trace length affects 2 important parameters, namely Capacitance and Signal Delay Time.
- Micro stripe Line

  2.76pF/in

  140ps/in
- Stripe line

  3.6pF/in

  170-180ps/in



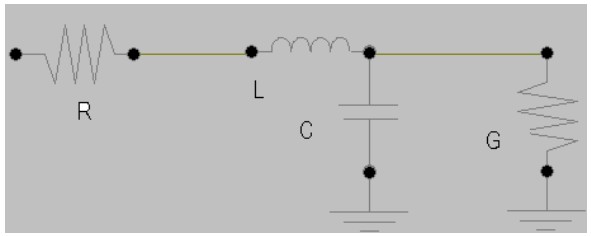
Characteristic Impedance

The impedance of transmission Line is :

$Z = ((R+jwL)/(G+jwC))^{1/2}$

Where R and G are the

Frequency dependent

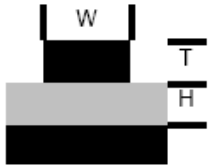


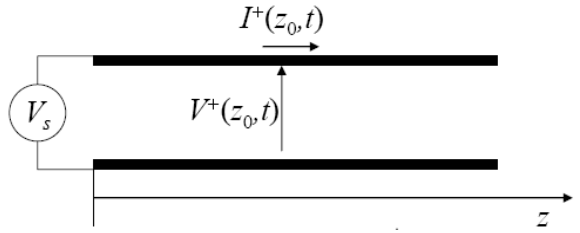
Microstrip

$$Z_0 = \frac{87}{\sqrt{Er+1.41}} Ln\left(\frac{5.98H}{.8W+T}\right)$$

$$C_0 = \frac{.67\,(Er+1.41)}{Ln\,[5.98\,H\ /(.8W\ +T)]}$$

$$t_{pd} = 1.017\sqrt{.475Er+.67}$$





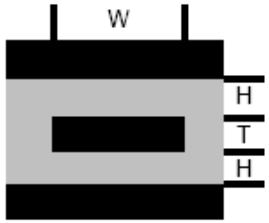
$$\frac{V^+(z,t)}{I^+(z,t)}$$

Stripline

$$Z_0 = \frac{60}{\sqrt{Er}} Ln\left(\frac{1.9(2H+T)}{(.8W+T)}\right)$$

$$C_0 = \frac{1.41\,Er}{Ln\,[3.81\,H\ /(.8W\ +T)]}$$

$$t_{pd} = 1.017\ \sqrt{Er}$$



$$Zo = \sqrt{\frac{Lo}{Co}} + Ro \text{ Ohms}$$

$$Zo = \sqrt{\frac{Lo}{Co}} \text{ Ohms}$$

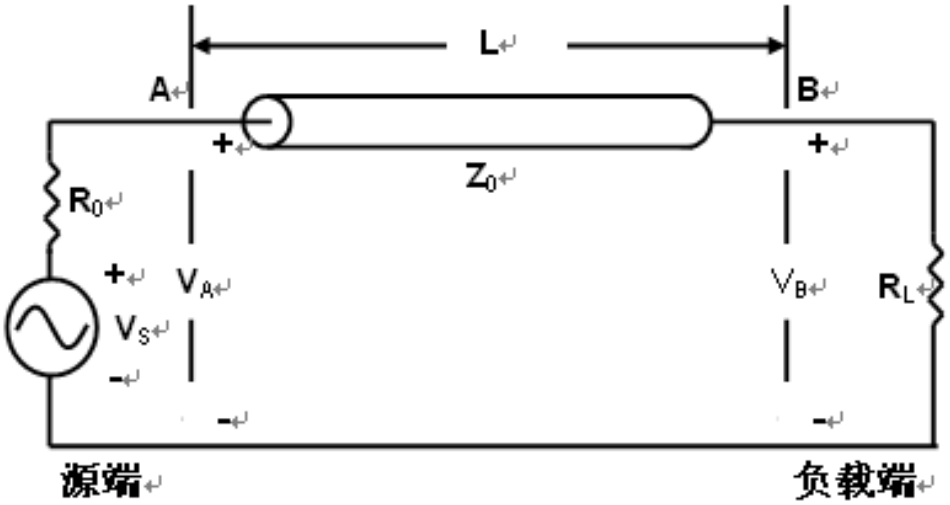
Characteristic Impedance

- The characteristic impedance of trace must match that of the tester.(most modern testers are 50 Ohms)
- If trace and tester impedance do not match there will be reflection noise.
- The general requirement is +/-10% tolerance, but for high speed testing we shall design +/-5% tolerance.

Reason of effect signal performance

- Reflection
- Delay
- Loss
- Cross Talk
- Ground Bounce/Power Bounce

Reflection



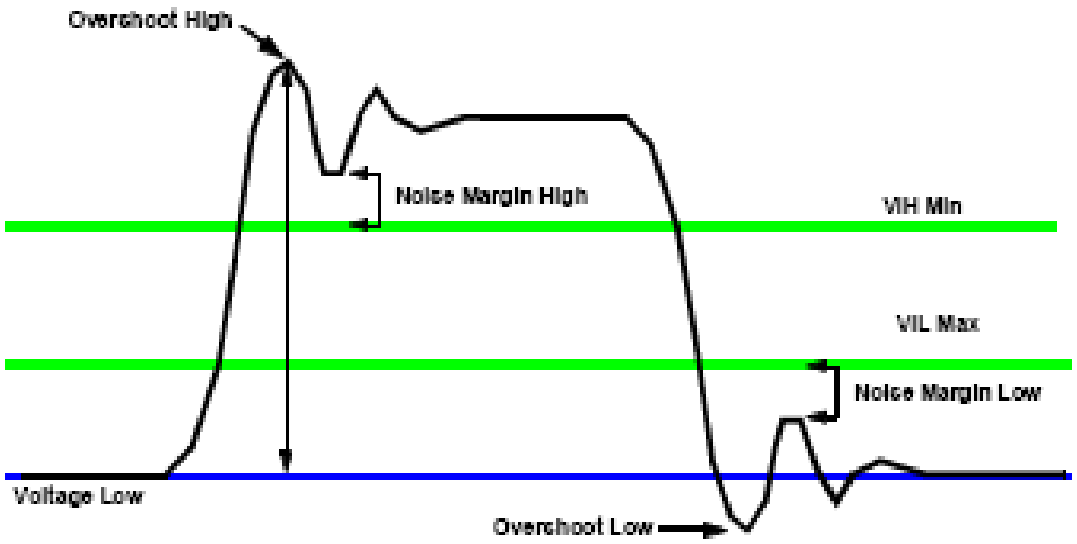
理想传输线模型及相关参数

$$\rho_L = \frac{R_L - Z_0}{R_L + Z_0}$$

$$\rho_S = \frac{R_0 - Z_0}{R_0 + Z_0}$$

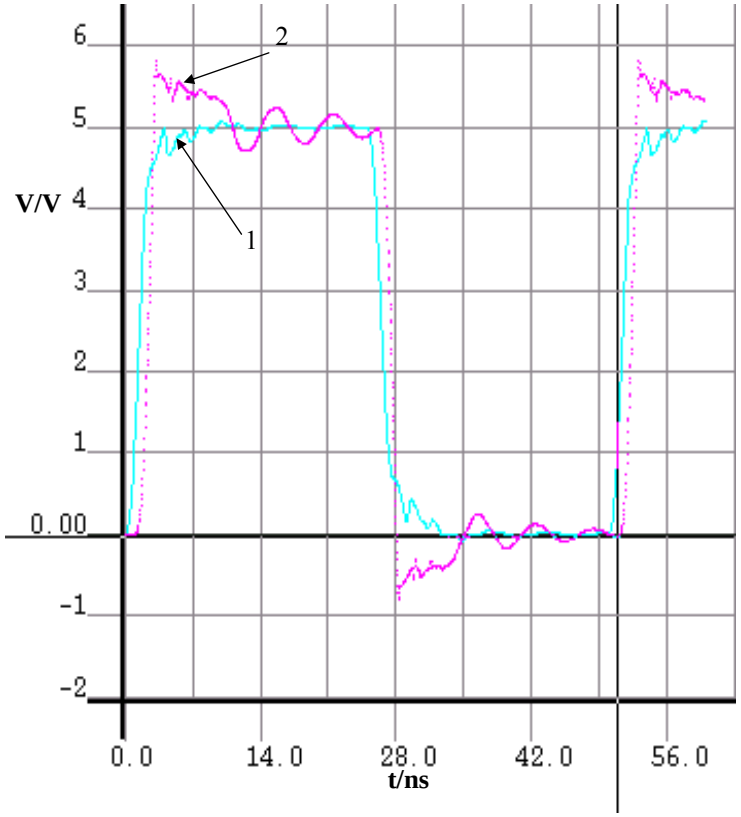
R0＝Z0＝RL, no any refection, but it is impossible.

Reflection



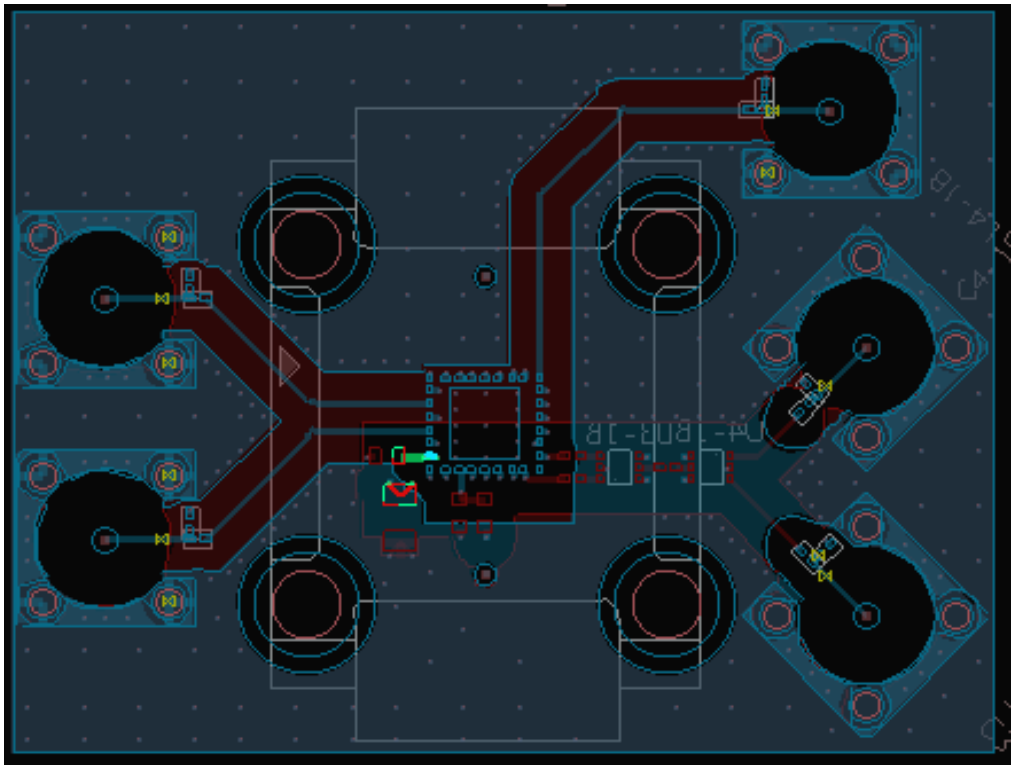
Terminology Translation

Cadence	A.K.A
Overshoot (Rising Edge)	Overshoot
Overshoot (Falling Edge)	Undershoot



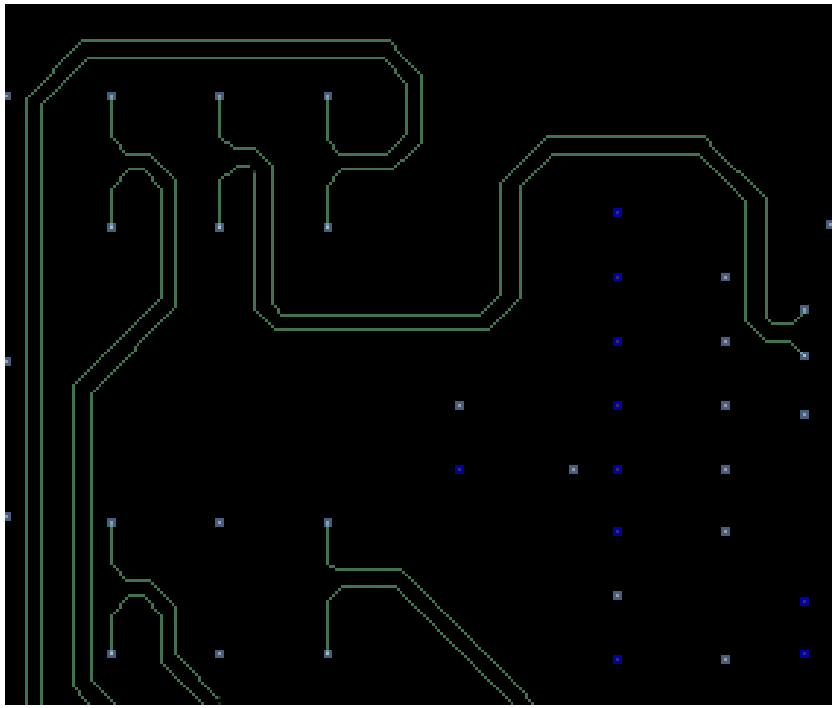
Ring

Affect the trace impedance elements



RF traces Almost the same width with pads

Differential Impedance



Loose coupling differential pairs for easy to control differential impedance .

Ideal Canculate

Impedance

Cross Section

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Impedance (ohm)
21		DIELECTRIC	FR-4	5	0	4.000000	0.035				
22	L11_PWR3	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
23		DIELECTRIC	FR-4	4	0	4.000000	0.035				
24	L12_GND6	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
25		DIELECTRIC	FR-4	5	0	4.000000	0.035				
26	L13_PWR4	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
27		DIELECTRIC	FR-4	4	0	4.000000	0.035				
28	L14_GND7	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
29		DIELECTRIC	FR-4	5	0	4.000000	0.035				
30	L15_PWR5	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
31		DIELECTRIC	FR-4	4	0	4.000000	0.035				
32	L16_PWR6	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
33		DIELECTRIC	FR-4	5	0	4.000000	0.035				
34	L17_GND8	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
35		DIELECTRIC	FR-4	7	0	4.000000	0.035				
36	L18_S3	CONDUCTOR	COPPER	1	595900	1.000000	0	☐		6.000	52.198
37		DIELECTRIC	FR-4	7	0	4.000000	0.035				
38	L19_GND9	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
39		DIELECTRIC	FR-4	7	0	4.000000	0.035				
40	L20_S4	CONDUCTOR	COPPER	1	595900	1.000000	0	☐		6.000	52.198
41		DIELECTRIC	FR-4	7	0	4.000000	0.035				
42	L21_GND10	PLANE	COPPER	1	595900	1.000000	0	☒	☒		
43		DIELECTRIC	FR-4	4.7	0	4.000000	0.035				
44	BOTTOM	CONDUCTOR	COPPER	2	595900	1.000000	0	☐		8.000	51.634
45		SURFACE	AIR								

Total Thickness: 145.4 MIL

Initialize Conductive Layer Dielectric: [Custom Values]

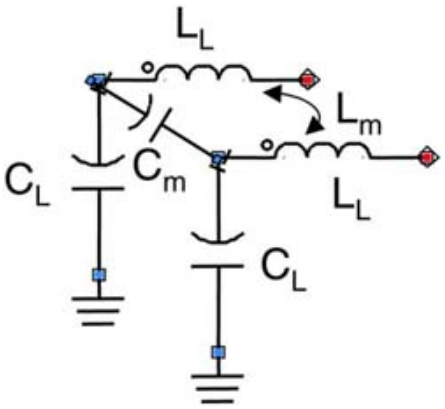
Dielectric Constant:

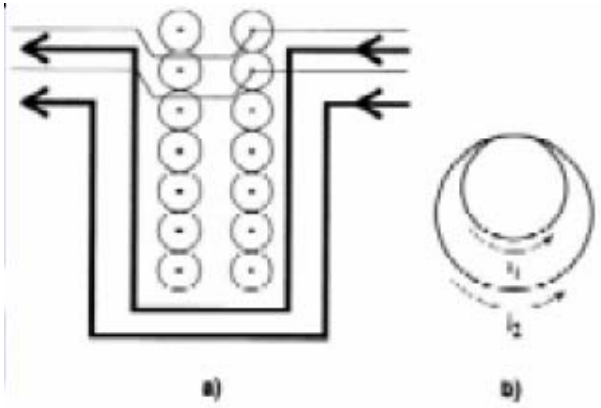
Loss Tangent:

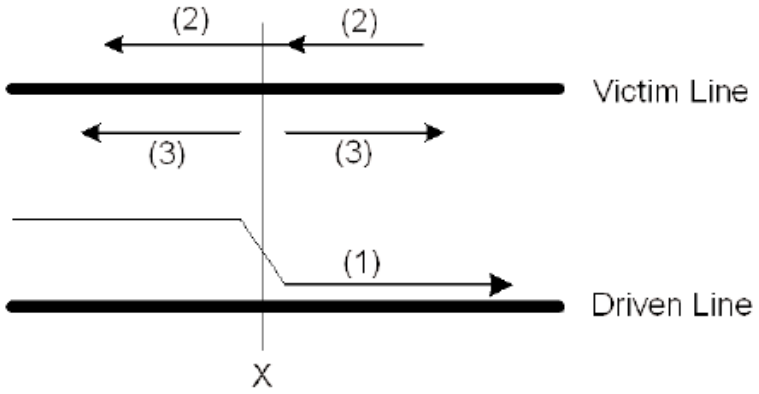
☐ Differential Mode

cross talk

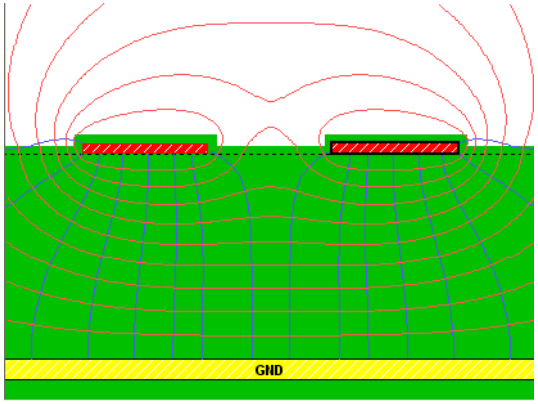
- Capacitance Crosstalk
- Inductance Crosstalk
- Loop Noise



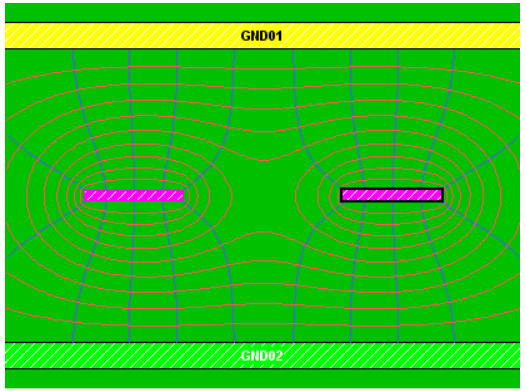


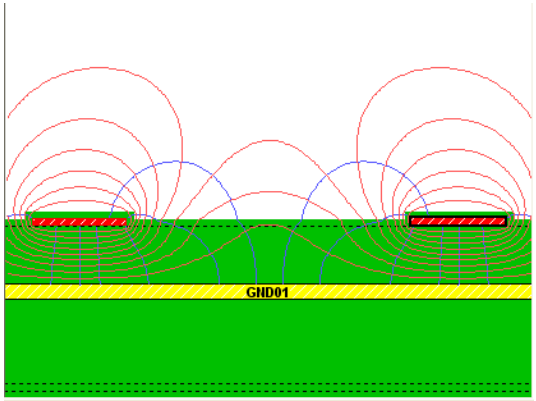


cross talk

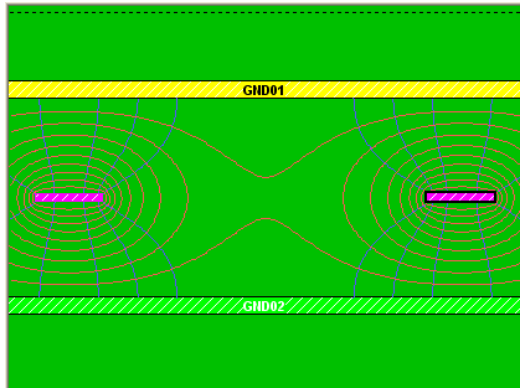


Edge to Edge 1 W





Edge to Edge 3 W



Power Design

PI：

- High switch current
- Inductance parameters in circuit

Target Impedance

$$Ztarget = \frac{(V0) \text{ X } (a\%)}{Imax}$$

- Ground Bounce
  Power Bounce
  SSN (Simultaneous Switch Noise)

$$Ztarget = \frac{3.3V \text{ X } 5\%}{1A}$$

$$= 0.165\ \Omega$$

$$Vdrop = iR + L\ di/dt$$

Power Design

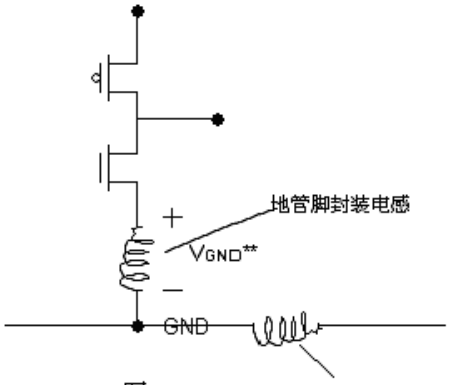


图1-a 非理想地平面存在阻抗

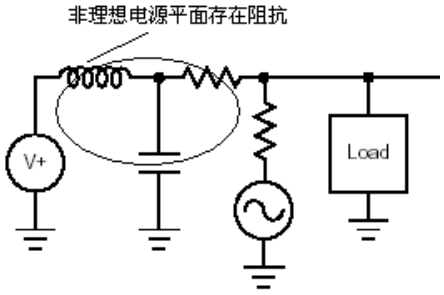


图1-b

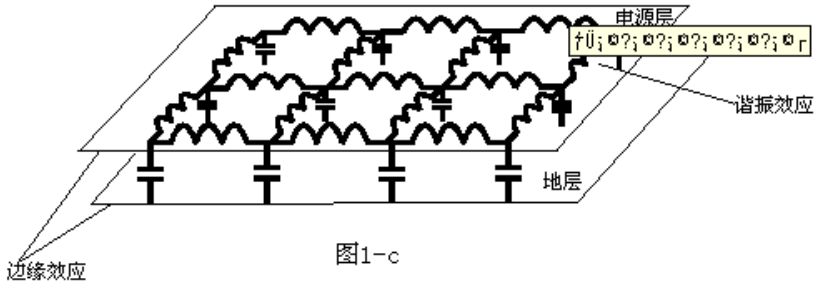
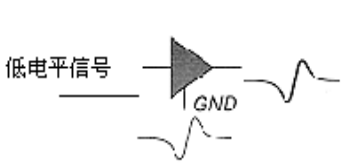
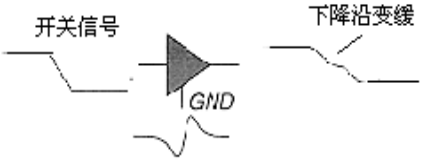


图1-c

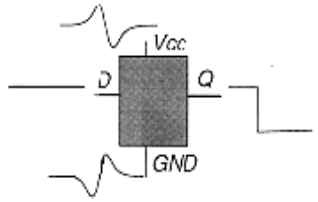




a 地弹噪声对驱动端信号的影响

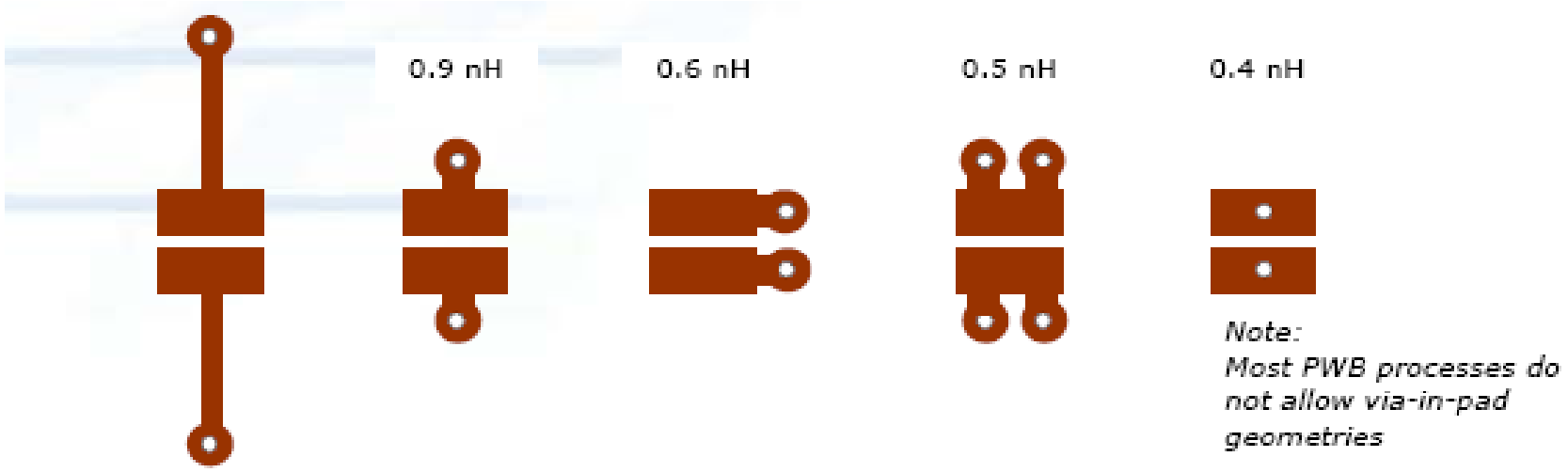
地弹噪声对接收端信号的影响

b



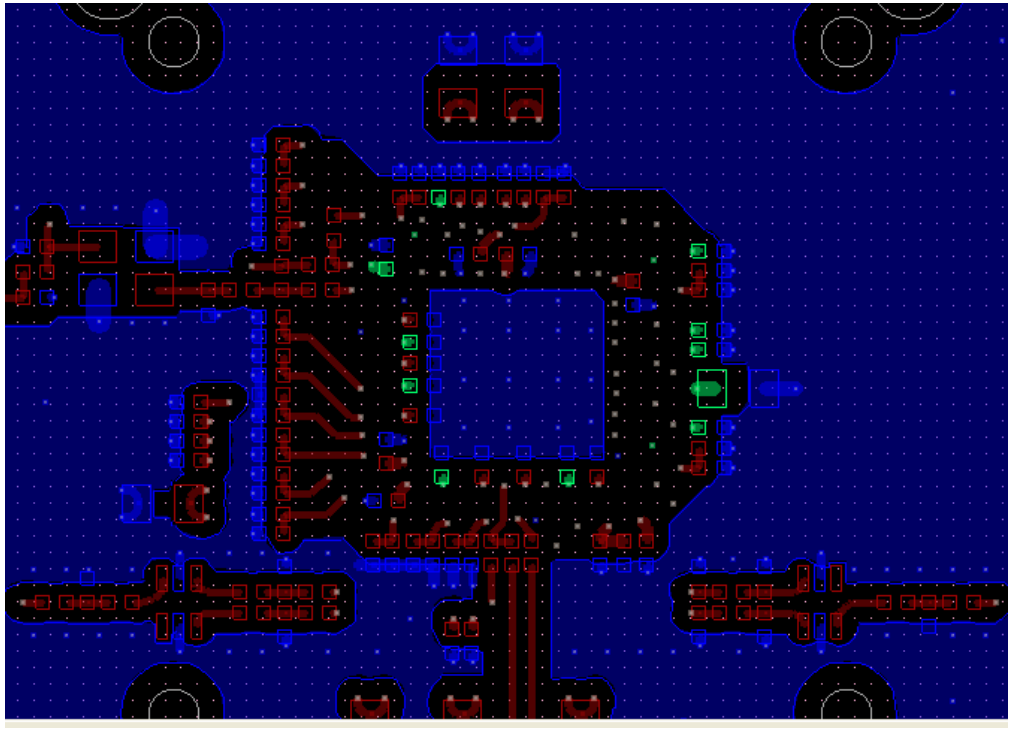
C 触发器数据翻转

Power Design



Power Integrate

Via On PADS, No trace used from Caps pads



Part 3 PCB Material

Dk
Dielectric Constant

Tg
Glass Transition Temperature

Df
Dissipation Factor
- Fr4: 0.015-0.022.
- 1GHz <=0.012.
- 3GHz <=0.004.

PCB material

- Insulectro- FR406, FR408, FR410, IS410,370HR LeadFree, Polymide-P95
- Nelco: N4000-6, N4000-11, N4000-13, N4000-13SI, N4000-13EP
- Nanya: NP170, NP175
- Getek: Getek
- Rogers: 3003, 3210, 3850, 4003, 4350, 6002
- Arlon: 85N, 25N, Cuclad

PCB material

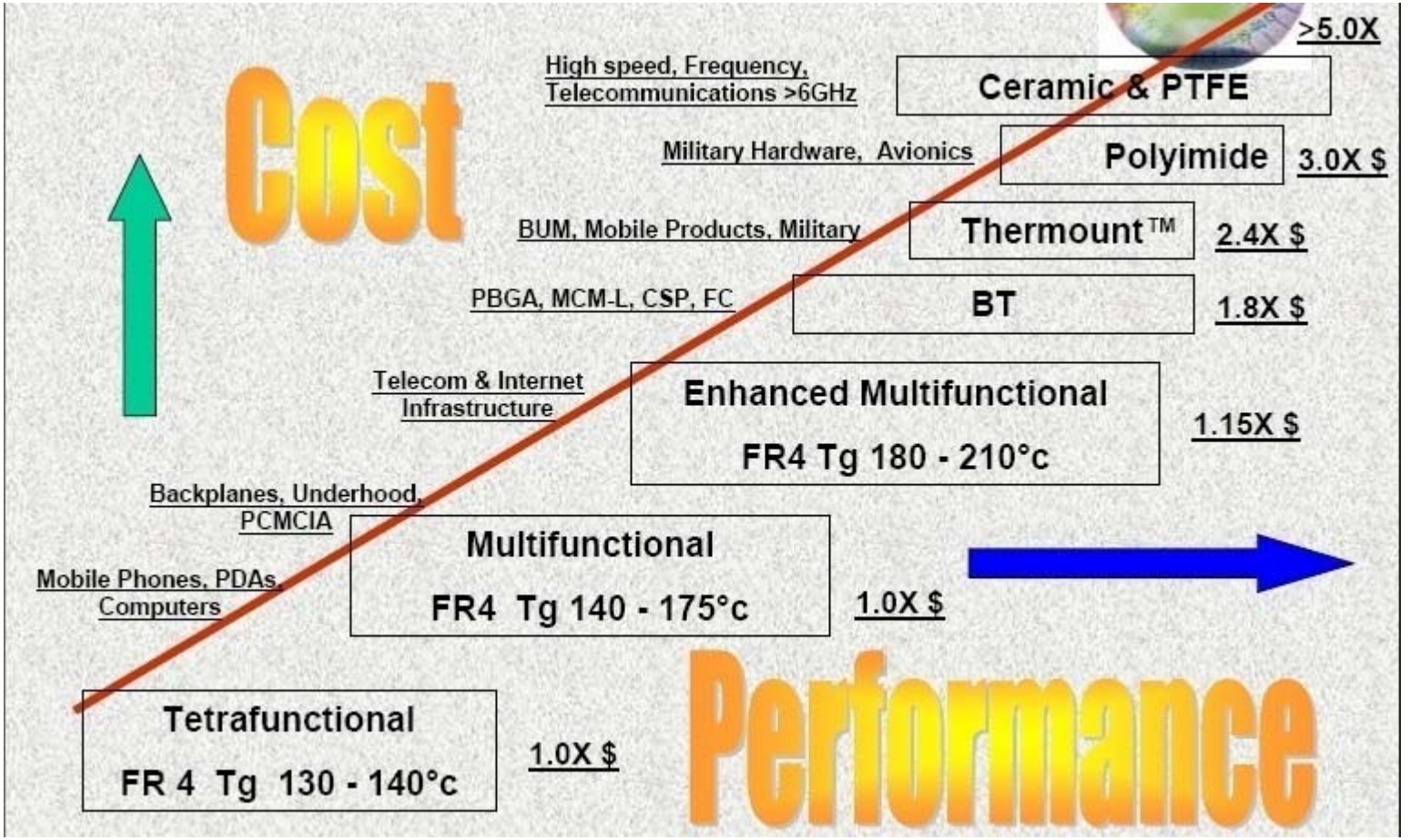
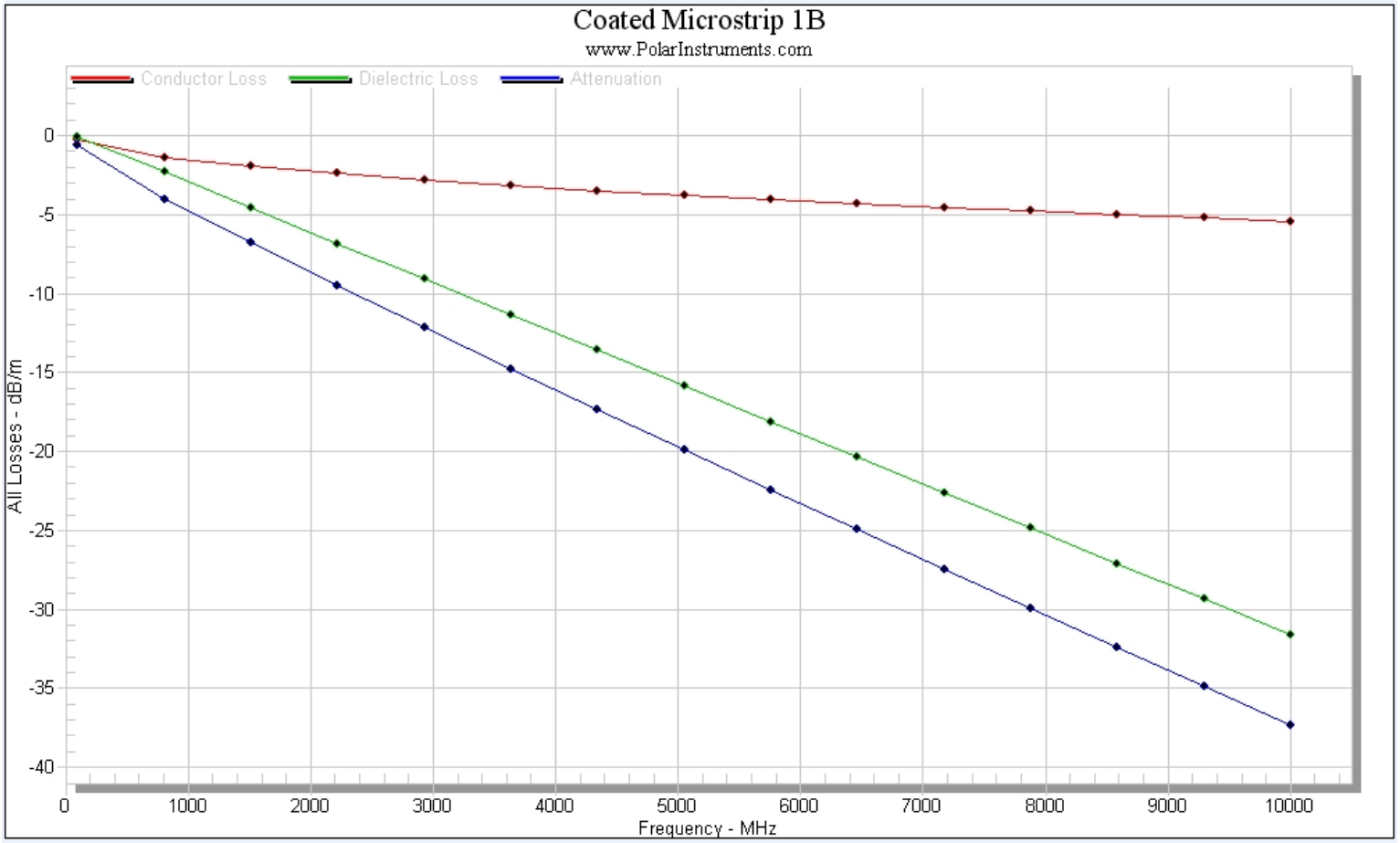


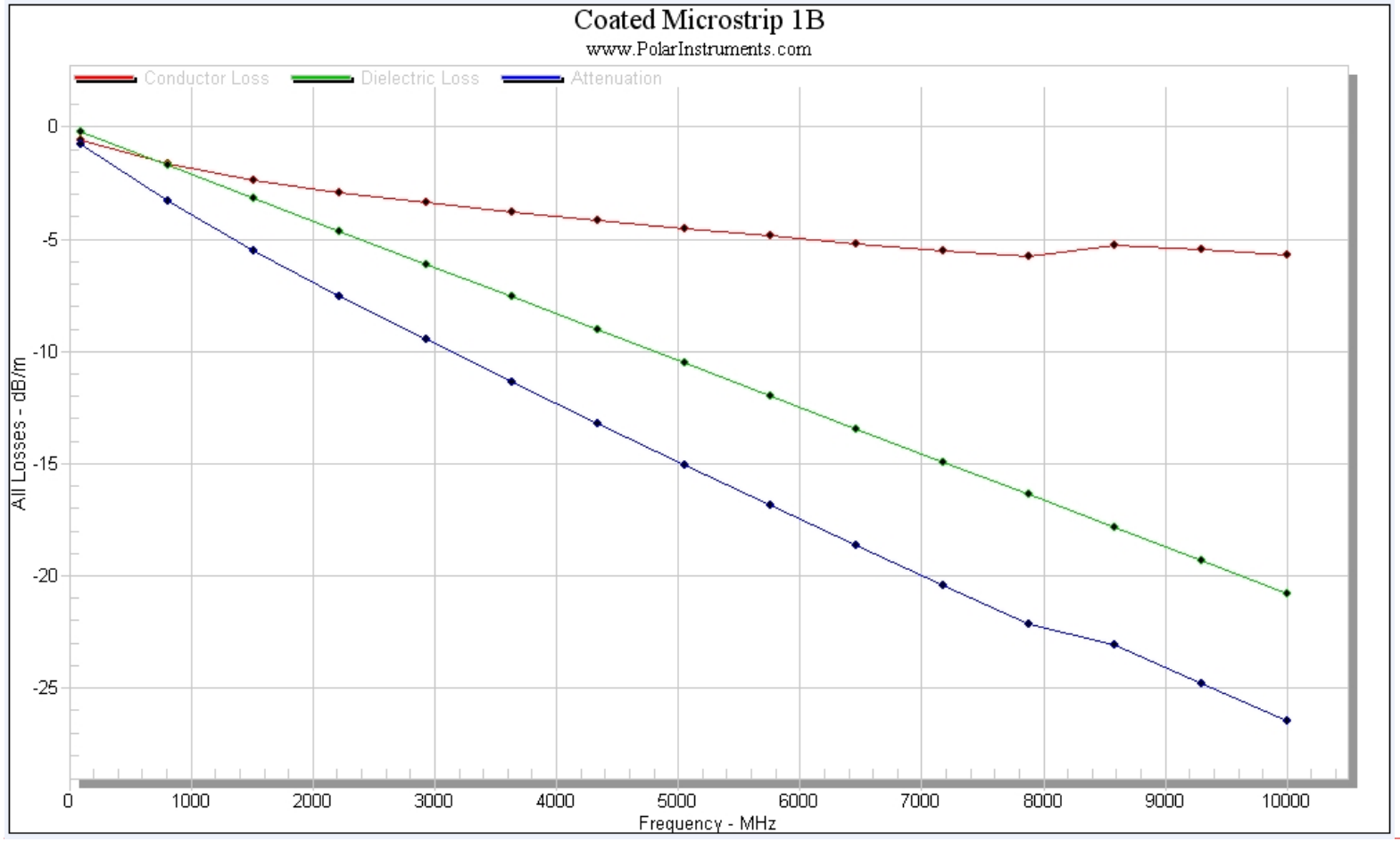
Table 19: Laminate Selection

Cost	Tg	Dk	Df	Use	Comments	Examples of materials (alphabetic)
Lowest ↓ Highest	*General Purpose*					
	FR4, Low Tg (125 - 135ºC)	4.3 - 4.7	0.03	General purpose	Difunctional FR4 epoxy laminate	Isola: FR402 Nelco: 4000-2
	FR4, Mid Tg (140 - 150ºC)	4.3 - 4.7	0.03	General purpose	Tetrafunctional FR4 epoxy laminates. More stable than low Tg.	Isola: FR404 Nelco: 4000-4 Polyclad: FR226
	FR4, High Tg (170 - 190ºC)	4.3 - 4.7	0.03	General purpose	Multifunctional FR4 epoxy laminates. More stable than mid Tg.	Isola: FR406 Nelco: 4000-6 Polyclad: FR370
	Enhanced Performance Materials for High Speed/Low Loss Applications					
	FR4+ (190 - 220ºC)	3.7 - 3.9	0.012	High speed applications	Lower Dk (Dielectric Constant) and lower Df (Loss Tangent) than FR4.	Isola: GEtek / Megtron FR408 Nelco: N4000-13 BT Laminates: PR370 Turbo
	PTFE ~ 220ºC	2.6	0.004	Very high speed applications	Lower Dk and Df losses than above. PTFE, No glass	Gore: Speedboard Nelco: 9000
	CE~ 250ºC	3.7	0.011	High temperature applications	Cyanide Ester	Nelco:8000
	RF Applications					
	Ceramic filler + core material >200ºC	3.3 - 3.8	0.004 - 0.009	RF Applications	Usually used as an outer layer, laminated to FR4 for RF. A family of materials with a range of Dk and Df values	Rogers: 4350
	APPE ~ 210ºC	3.5	0.004	High speed applications	APPE - Allyled PolyPhenylene Ether	Megatron 5 Nelco: N6000
	Military, Flex and Rigid Flex Applications					
	Polyimides >220ºC	3.8	0.015	High speed, Military and Flex	Absorbs moisture. Requires pre-baking	Nelco: N7000
	LCP ~ 280ºC	3.8	0.015	High speed and Flex applications	Liquid Crystal Polymer is dry	

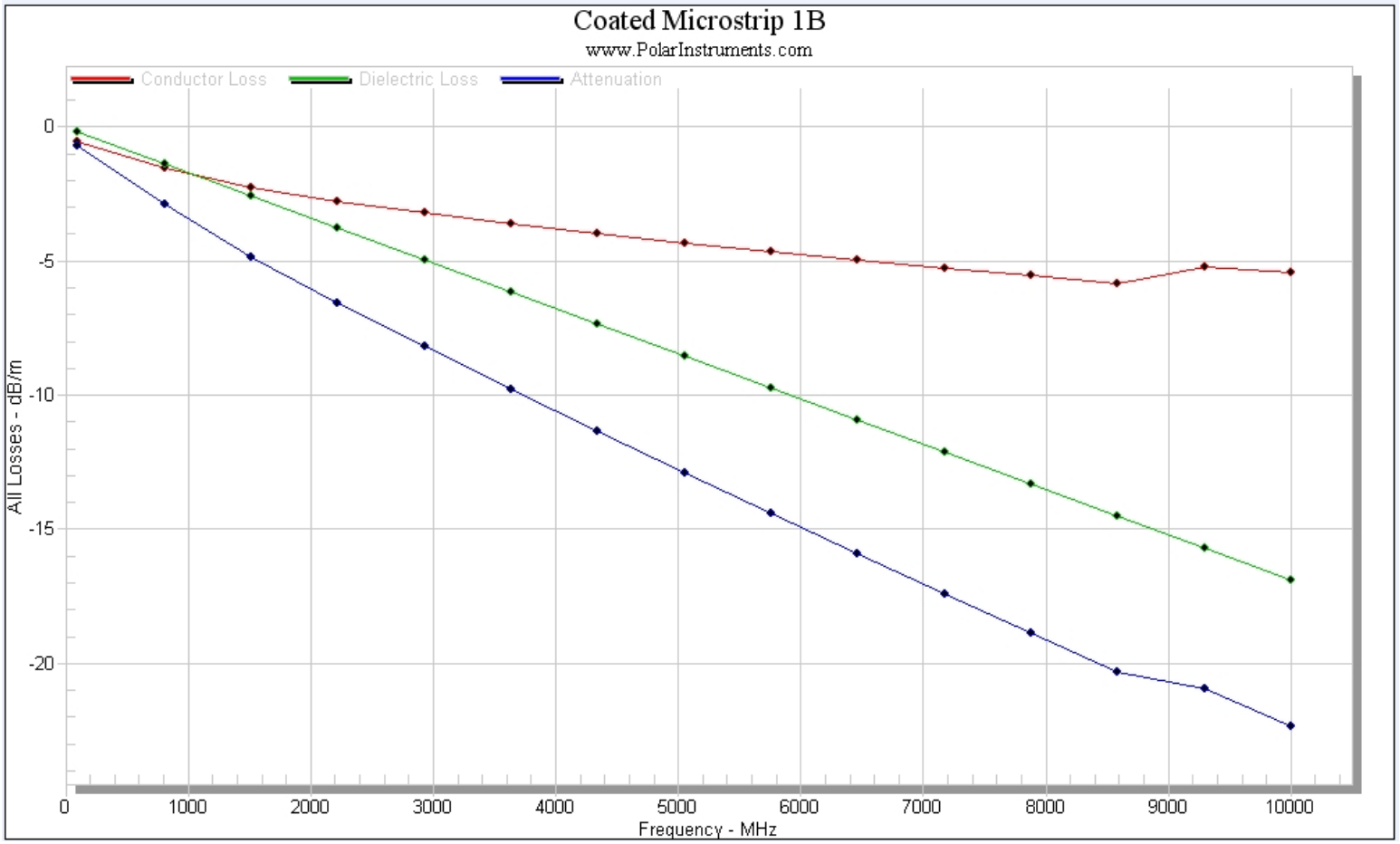
Standar FR4 (Er: 0.022)



FR406 (Er: 0.014)

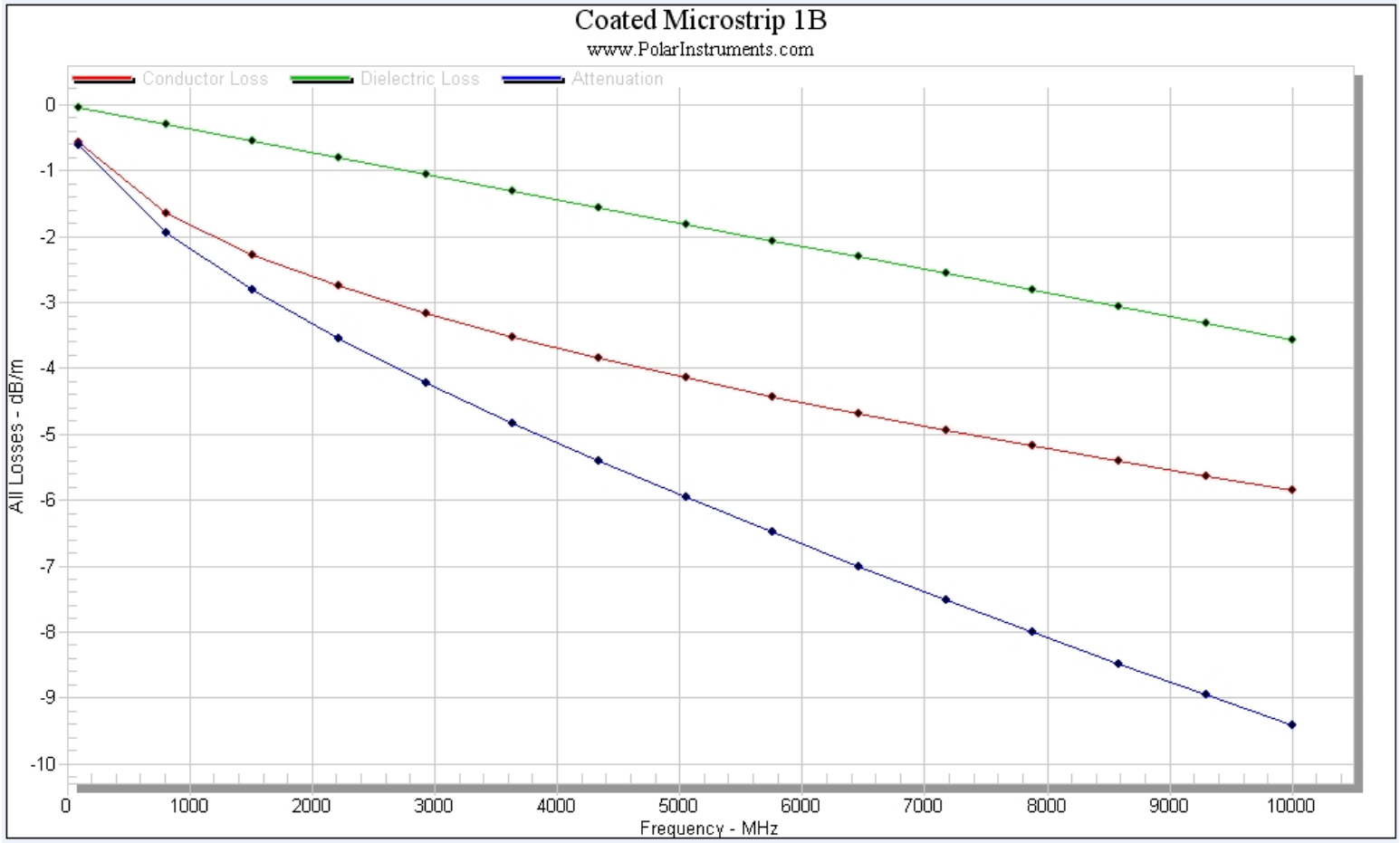


Getek (Getek_R Er: 0.012)



Virtuous

Rogers (RO4003 Er: 0.0027)



Part 4 PCB Manufacture

- Panel max Size (inch)

  14 X 16

  16 X 22

  19 x 24

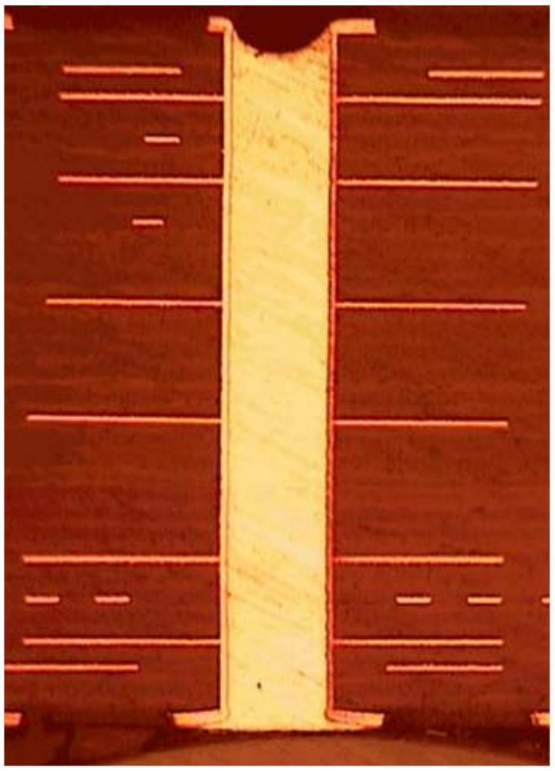
  22 x 22

  19 x 26

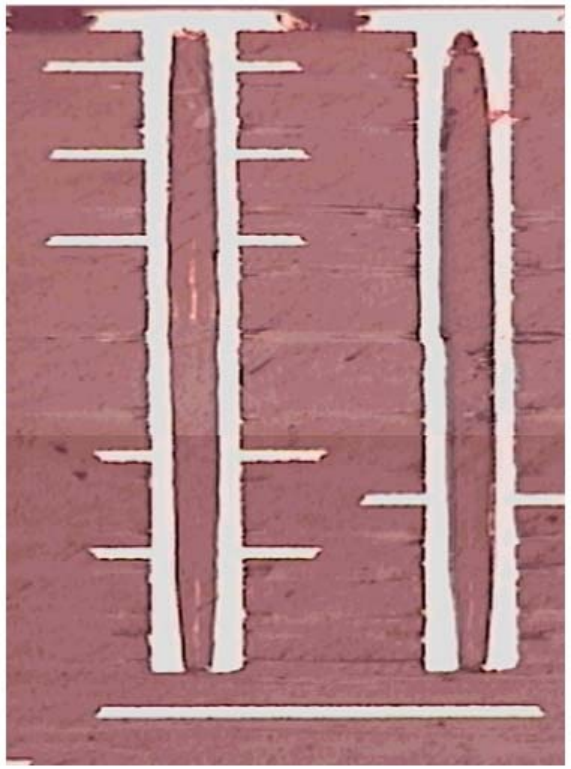
  22 x 26

Drill Information

Through Hole

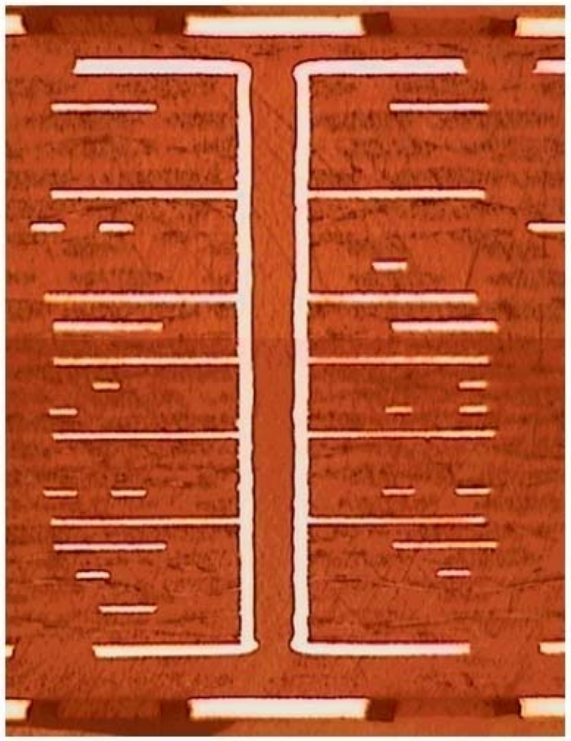


Blind Via

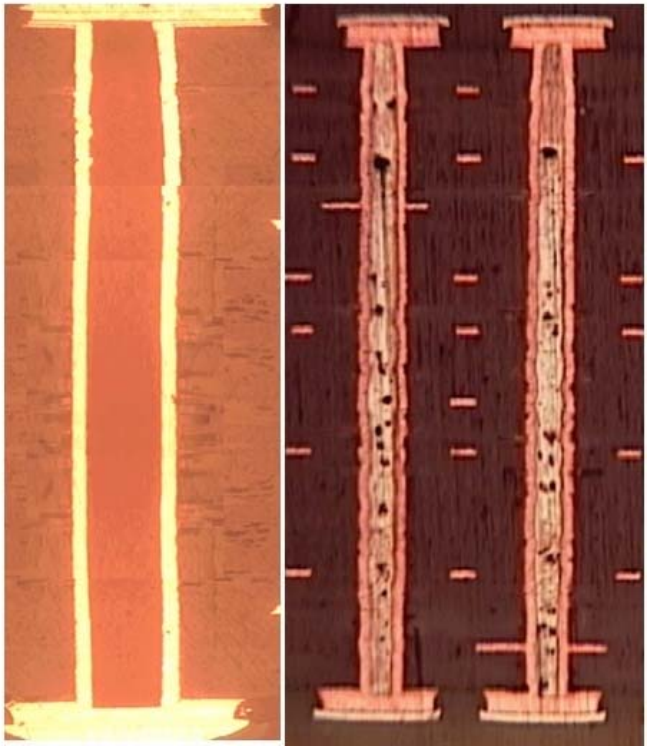


Drill information

Buried Via

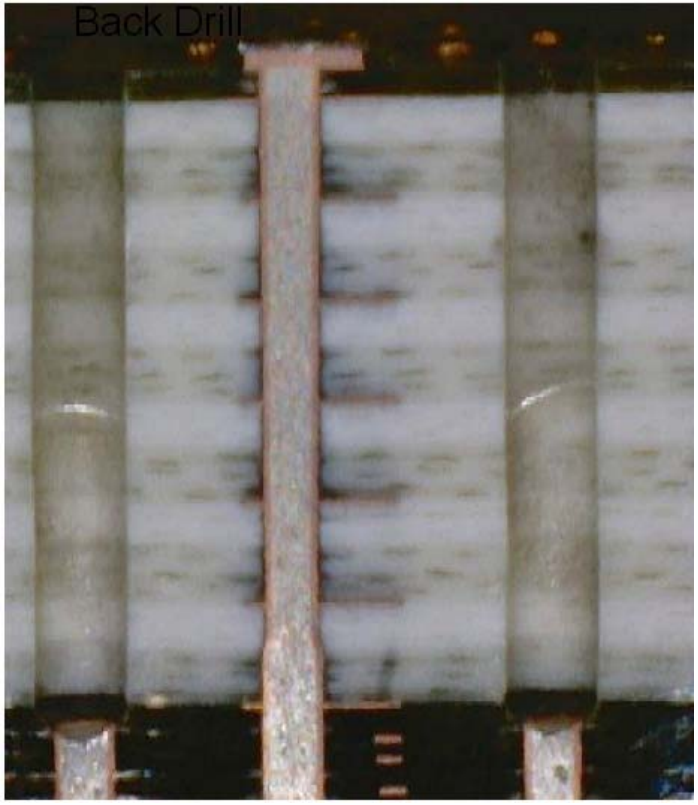


Conductive/No-Conductive Via



Drill information

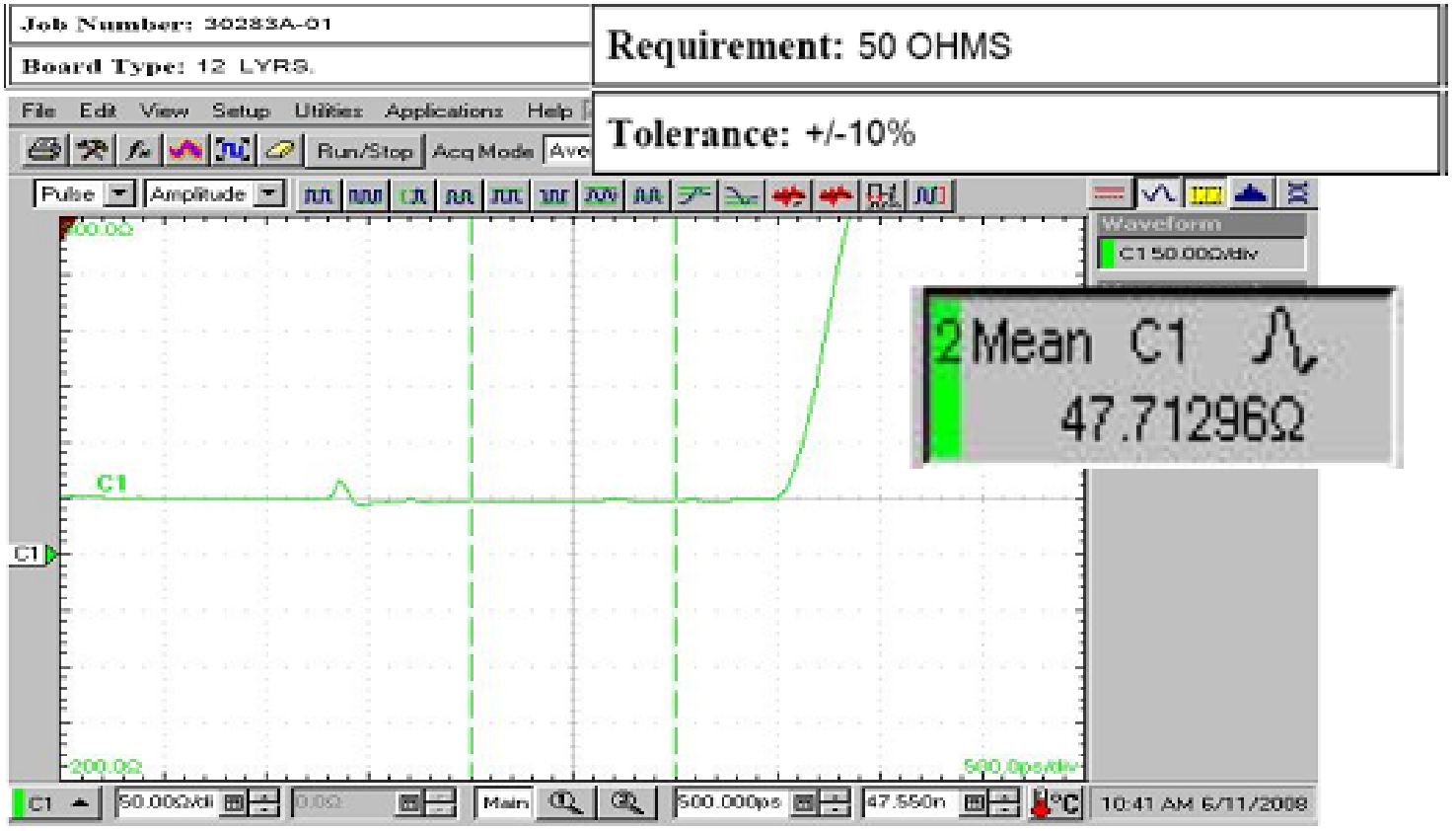
Back Drill



Surface finish

- HASL
- OSP
- Immersion Gold (8-10 µinches)
- Electrolytic Gold (20-50 µinches)
- Tab Plated Hard Gold over Nickel(5-100 µinches)
- Immersion Tin
- Immersion Siliver(8-18 µinches)

Impedance test



Electrical Test

- Flying Probe Test

  Minimum Space： 4 mil

  Minimum via/pad: 2 mil

  Short: 10 V 10 M Ohms

  Open: 10 V 10 Ohms

- High Voltage

  Short： 250 V 500 M Ohms

Trace Via and Ration

Trace width and Space		
Cu Foil	Stripe line	Micro stripe line
½ oz.	3.5/3.5	3/4.5
1 oz.	4/4.5	4/4.75
2 oz.	6/7	6/7

Ration(unit：mil)					
Via	4	5.9	7.9	12	14.5
Thickness	62	150	187	250	250
Advance	72	187	210	250	250
Ration	20:1	31:1	26:1	21:1	17:1

Conduct width/space	**Standard**	**Advanced**
Drill to Cu Space	8	5.5
Min Annular Ring inner layer	8	5
Min Annular Ring outer layer	6	4
Min Plane clearance inner layer	10	8
Min plane clearance outer layer	8	5

Mechanical Precision

- Thickness
  Max: Normal 187 mil Advance 250 mil
  Mini: Normal 25 mil Advance 15 mil
  Tolerance: Normal 10% Advance 5%
- Via/Hole Tolerance
  Plated hole: Normal +/-3 mil Advance +/-2 mil
  Unplated hole: Normal +/-3 mil Advance +/-2 mil
  XY Precision: Normal +/-1.5 mil Advance +/-1 mil
- Back Drill Tolerance: +10 mil
- Outline Tolerance: +/-10mil
- Bend: Normal 10 mil/inch Advance 3 mil/inch
- Ration: Normal 16:1 Advance 31:1

THANKS AND QUESTION