D10 Application Training

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D10 Training Outline

- Day1:
  - Plateform Overview
  - Timing And STIL
  - Passive Load
  - Instrument Pin Introduction
  - Program Overview(.job, .res, .sig, user_main, user_load, API etc)
- Day2:
  - Lab: ITE Environment
  - Lab: Run the Program
  - Lab: Run the Tool(shmoo, margin, pattern tool etc)
  - Frequency Measurement
  - To Use the DIBU

D10 Training Outline

- Day3:
  - Lab: Write your own test program (74193)
  - Binning
  - OIC

D-10 Technical Overview

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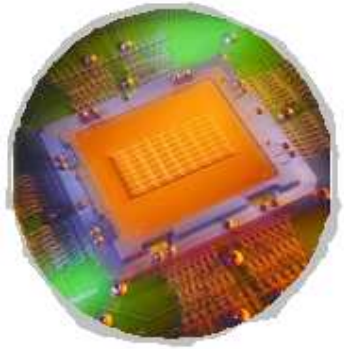
Use of Existing Technology

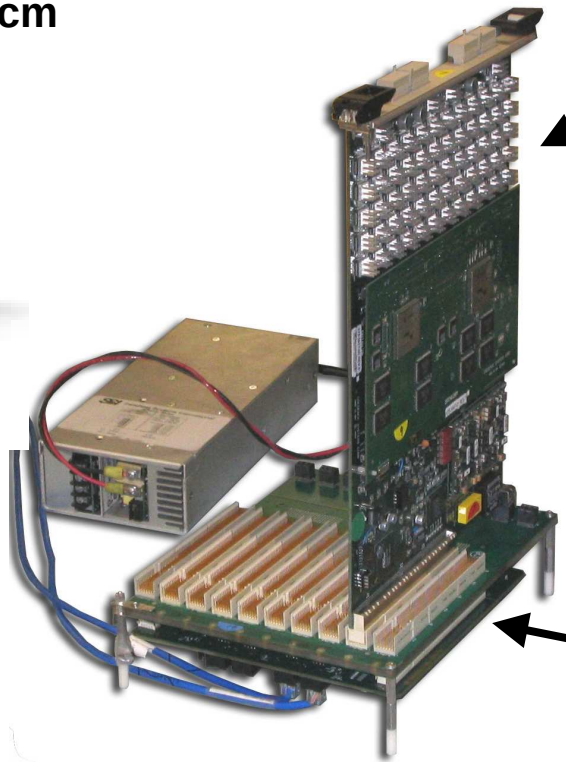
- Use of industry standards
  - STIL (Standard Tester Interface Language) Syntax
  - Star Fabric cPCI bridge to backplane
  - cPCI data bus interface
  - Third-party cPCI and PXI instruments
  - Third-party software tools
- Use of existing Credence technology
  - Omni ASIC for the DPIN96
  - Octet analog instruments for DMSI
  - Program Developer for program generation
  - Test Developer for pattern generation
  - Debug tools adapted from multiple platforms
  - VI technology from SZ
  - RF and Power Management technology from ASL

Architected for Performance



- Designed for multi-site
  - Sites management implemented in hardware for maximum throughput and minimum overhead
  - Multi-site analog and DC instruments
  - D-10 software designed for multi-site
- Designed for Maximum throughput
  - 250 Mbyte/s Star Fabric bridge for fast data transfers and pattern loads
  - FPGA based firmware algorithms implemented to accelerate throughput

Sapphire D-10



DPIN96

48V Power Supply

10 slot cPCI backplane

D-10 Digital / MS Instruments

Digital Pins

- 96 pins, 200Mbps
- 16M parallel vector memory, reconfigurable scan

Device Power

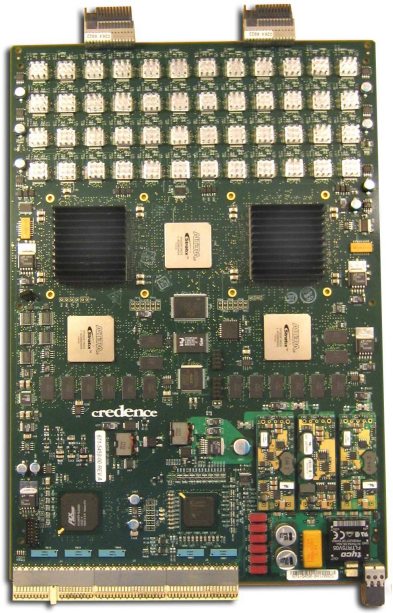
- 16 supplies
- 0 to +6V, 2A
- Gangable to 16A

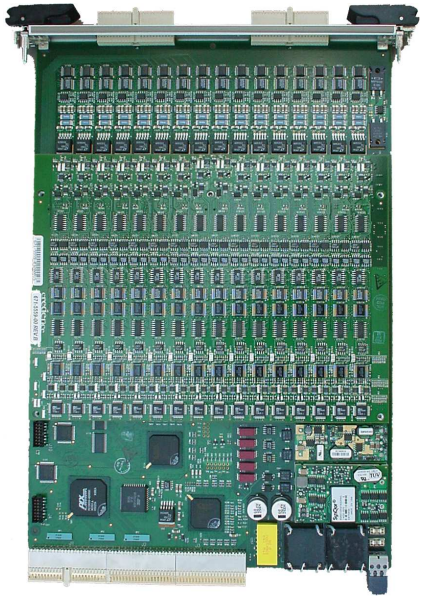
VI Sources

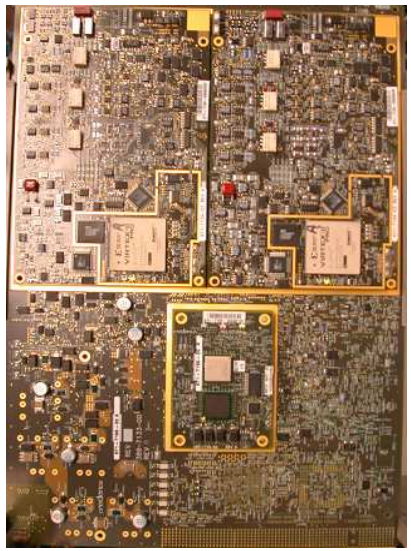
- 16 pins, 4 quadrant
- 20V, 300ma
- 60V, 100ma

Quad M/S Instruments

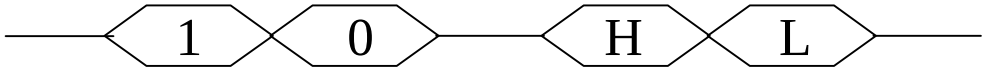
- Audio/Video AWG
- Audio/Video Digitizer





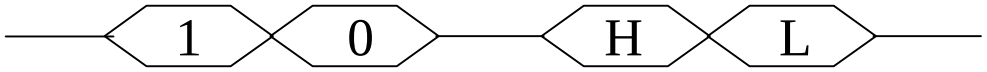


DPIN96 Digital Pincard



Feature	Diamond DPIN96
Channels per card	96
Max Drv or Cmp	200Mbps
Full Format I/O	200 Mbps
EPA	±500ps
Edge Resolution	19.5ps
Rise Time	1.2ns @ 3V
Drv Min Pulse	4ns @ 3V
Drv / Cmp Range	-1V to 6V
Drv Super Voltage	12V
Per Pin PMU	-2V to 12V, ± 25mA

DPIN96 Digital / Omni asic



Feature	Diamond DPIN96
Instruction Rate	100 MHz
Edges per pin	4
Data bits per pin	4
Time Sets: t1 t2 t3 t4 f1 f2 f3 f4	256 period (global) 256 edge per pin (global) 256 format per pin (global)
Memory Depth	16 Meg
Scan	Yes/Reconfigurable
Fail Capture	64 / 16 Meg

DPIN96 Timing

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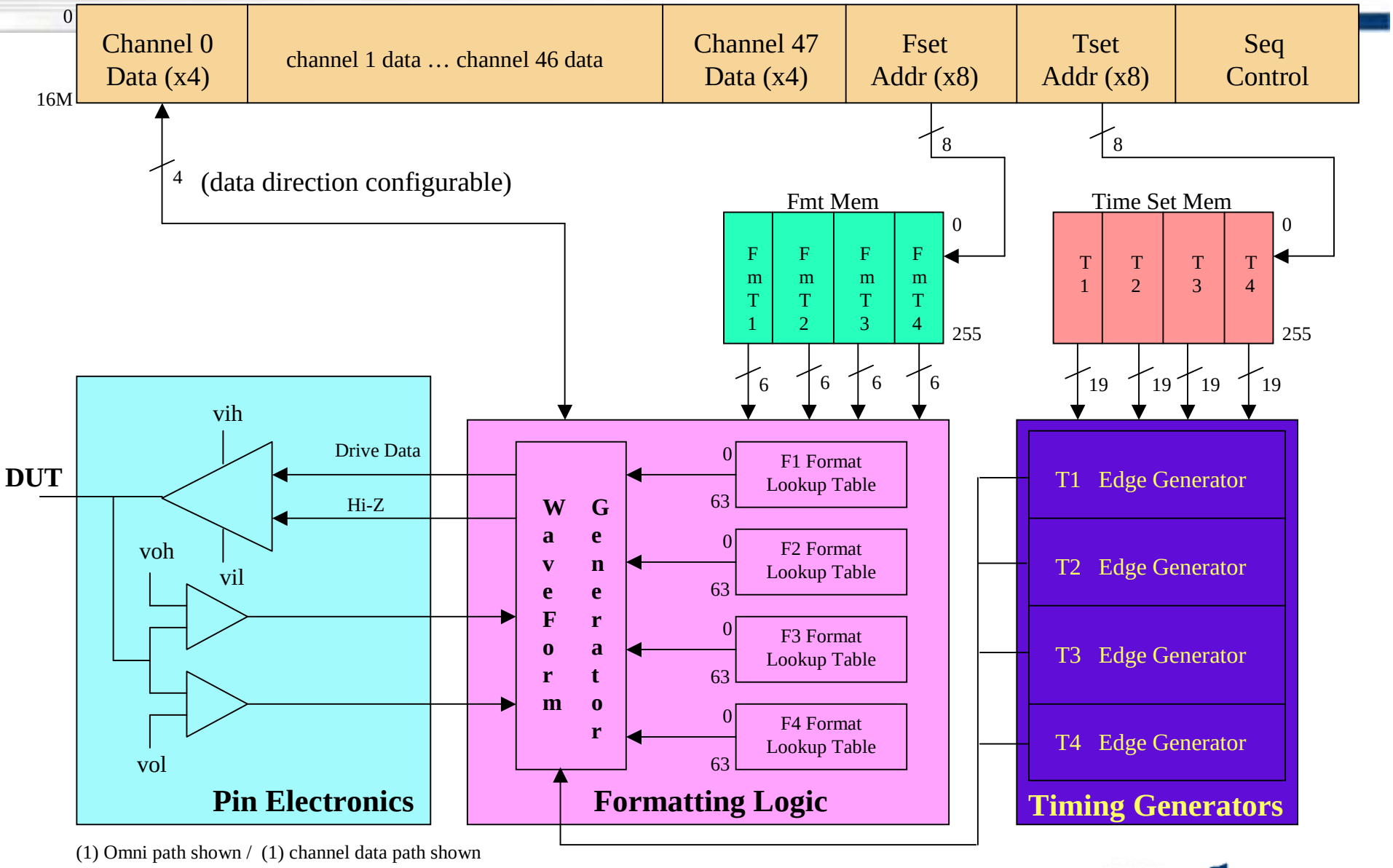
Vector Data Flow



(1) Omni path shown / (1) channel data path shown

Timing Examples in STIL

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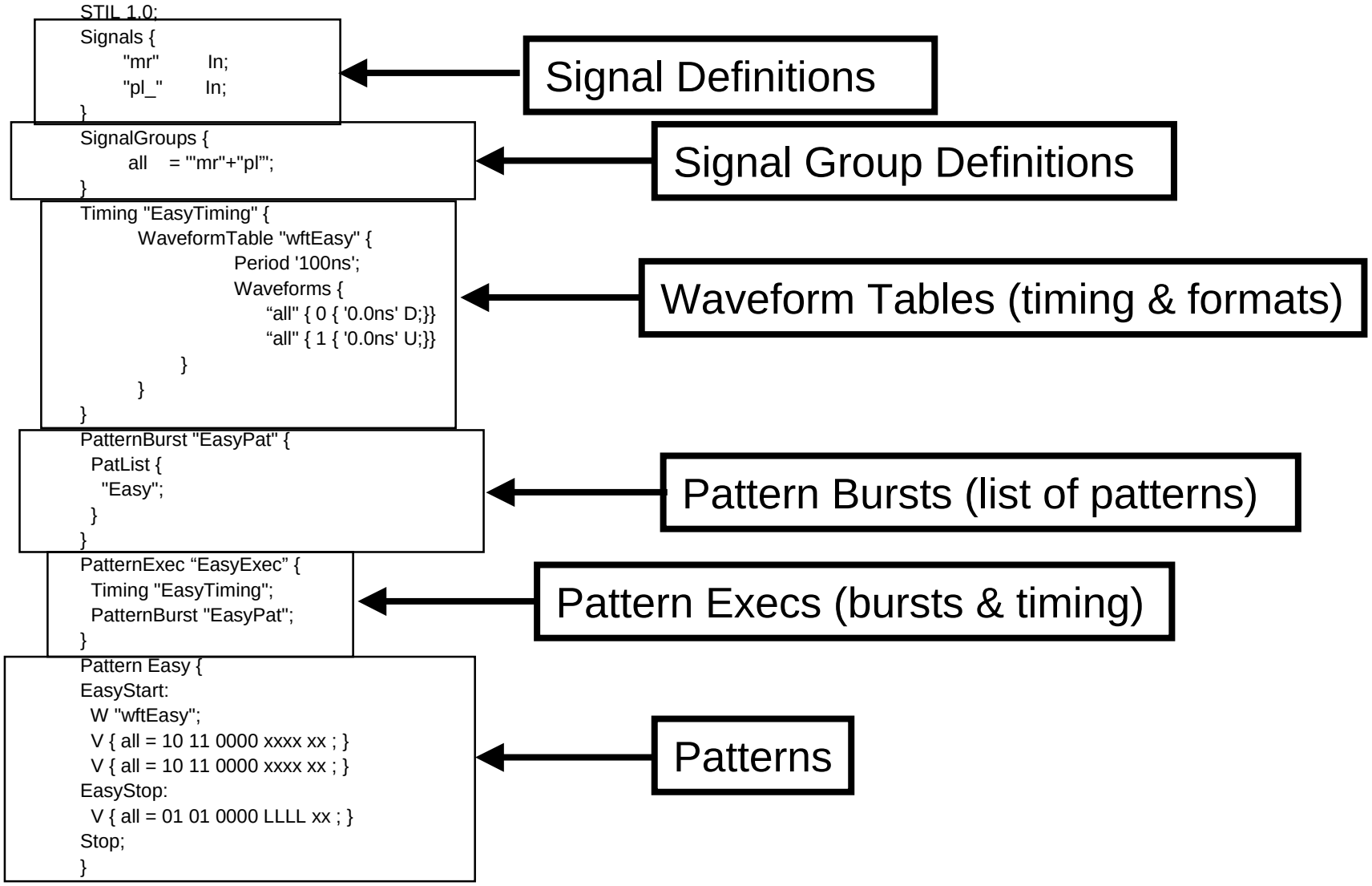
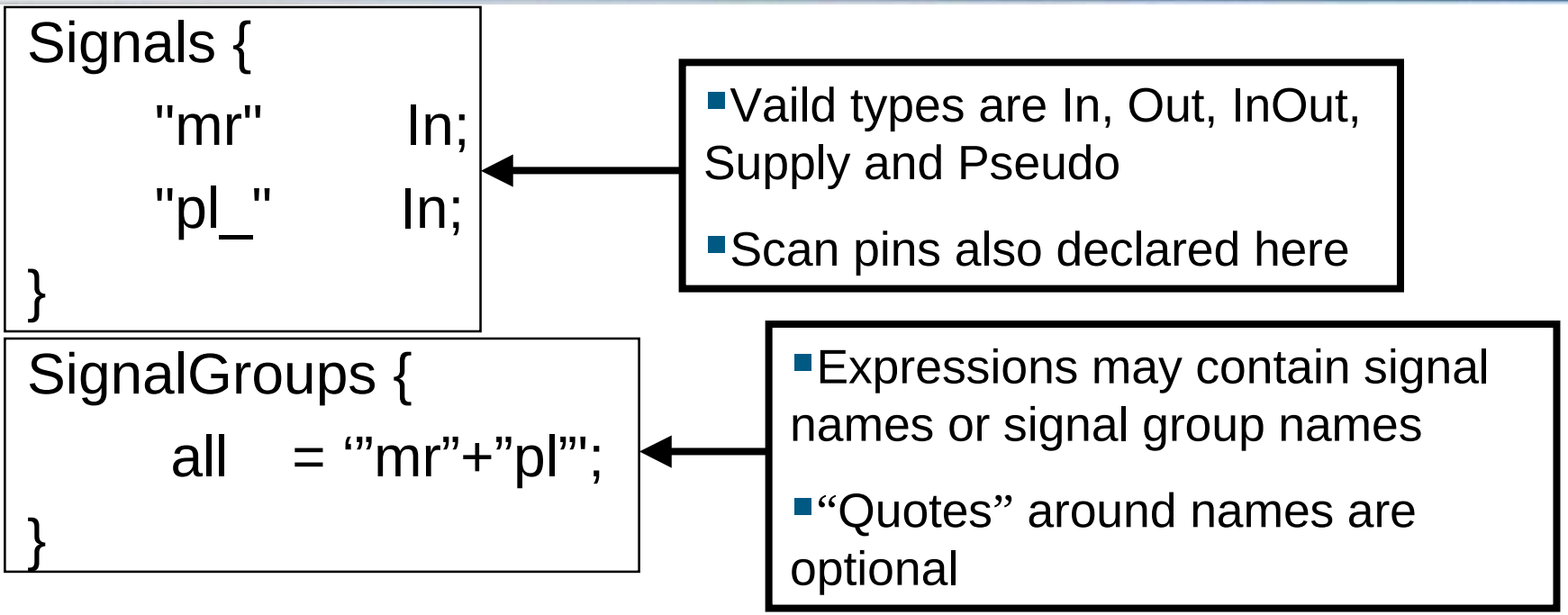
The STIL File



Signals and Signal List Definitions



See the Programmer's Reference Manual or the STIL IEEE spec for more information on STIL file syntax

Waveform Table Examples

```
Timing "EasyTiming" {
   WaveformTable "wftEasy" {
      Period '100ns';
      Waveforms {
            "dnrz_pins" { 0 { '5.0ns' D;}}
            "dnrz_pins" { 1 { '5.0ns' U;}}

            "r1_pins"   { 0 { '5.0ns' D; 55.0ns U;}}
            "r1_pins"   { 1 { '5.0ns' U;}}

            "rz_pins"   { 0 { '5.0ns' D;}}
            "rz_pins"   { 1 { '5.0ns' U; 55.0ns D;}}
         }
   }
}
```

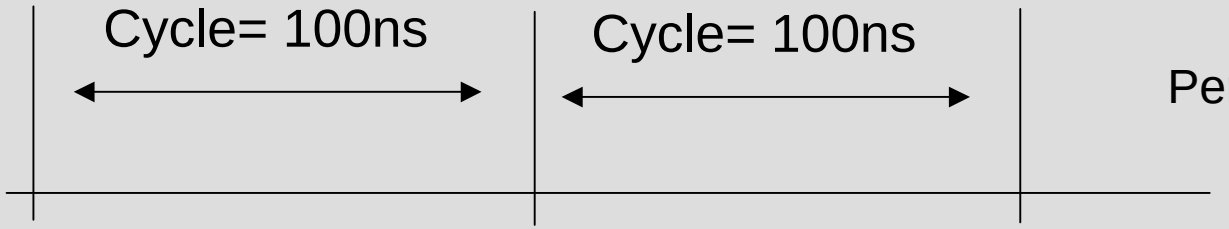
Tester period

Characters that will appear in the pattern

Description of waveform for each pattern character

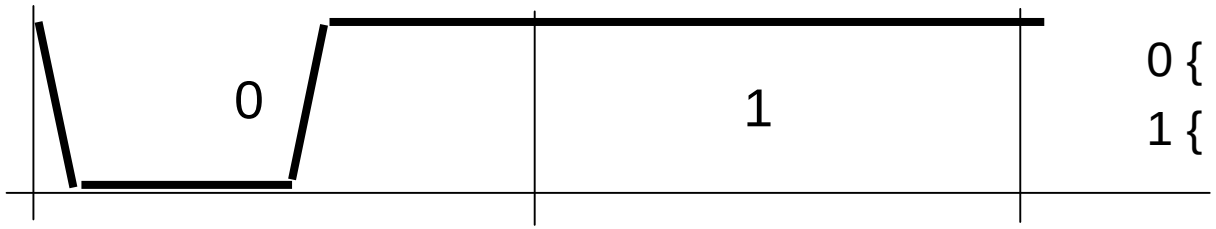
Signals or Signal Lists

Waveforms for Timing Examples



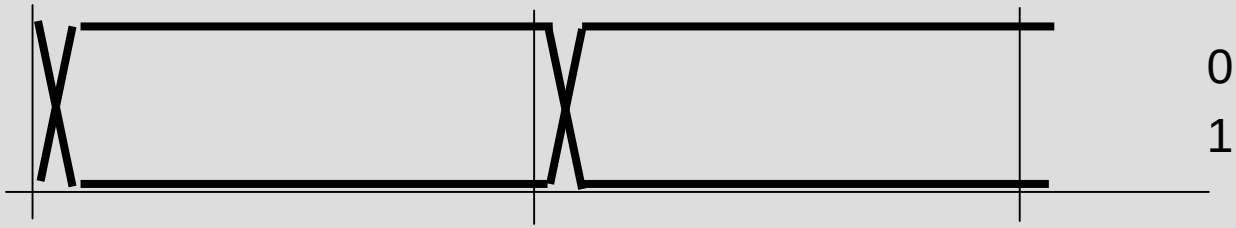
Period ‘100ns’;

R1



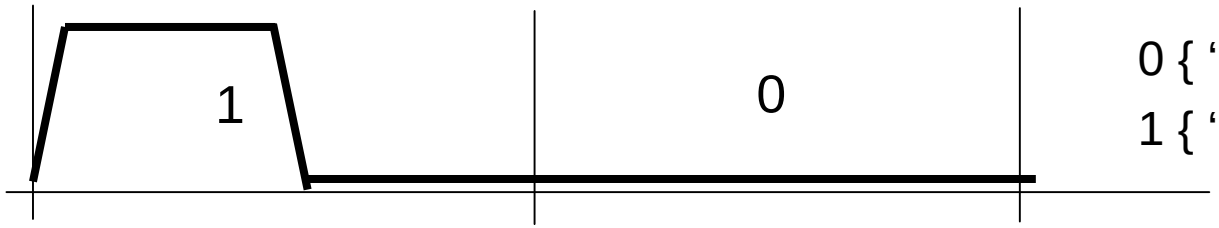
0 { ‘5.0ns' D; 55.0ns U;}
1 { ‘5.0ns' U;}

DNRZ



0 { ‘5.0ns' D;}
1 { ‘5.0ns' U;}

RZ



0 { ‘5.0ns' D;}
1 { ‘5.0ns' U; 55.0ns D;}

Four Edges Per Cycle

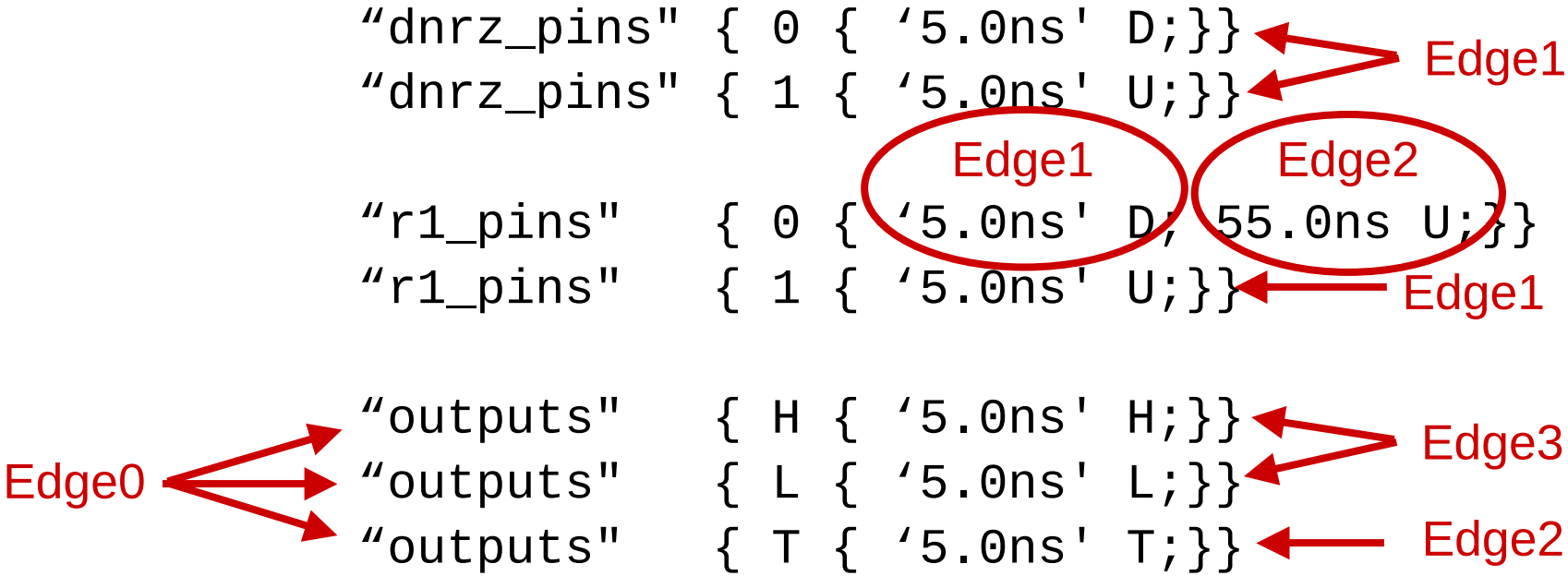
Edges	Edge 0	Edge 1	Edge 2	Edge 3
Events Allocated	X, Z	D, U, U1, N	D, U, U1, T, V, t, v	H, L, h, l

- The D-10 STIL compiler imposes some rules on the edge formats
- If not specified by defining ‘Z’ for a given signal, then the inhibit edge will default to 0ns
- Pattern states are:

Z= inhibit driver	X= mask
D= drive down	U= drive up
T,t= compare for tristate	V,v= compare for valid
H,h= compare for high	L,l= compare for low

Waveform Table Examples

```
Timing "EasyTiming" {
   WaveformTable "wftEasy" {
       Period '100ns';
       Waveforms {
             “dnrz_pins" { 0 { ‘5.0ns' D;}}
             “dnrz_pins" { 1 { ‘5.0ns' U;}}
             “r1_pins"   { 0 { ‘5.0ns' D; 55.0ns U;}}
             “r1_pins"   { 1 { ‘5.0ns' U;}}
             “outputs"   { H { ‘5.0ns' H;}}
             “outputs"   { L { ‘5.0ns' L;}}
             “outputs"   { T { ‘5.0ns' T;}}
          }
   }
}
```



The STIL File

```
PatternBurst "EasyPat" {
  PatList {
    "Easy";
  }
}
```

Pattern Bursts (list of patterns)

```
PatternExec “EasyExec” {
  Timing "EasyTiming";
  PatternBurst "EasyPat";
}
```

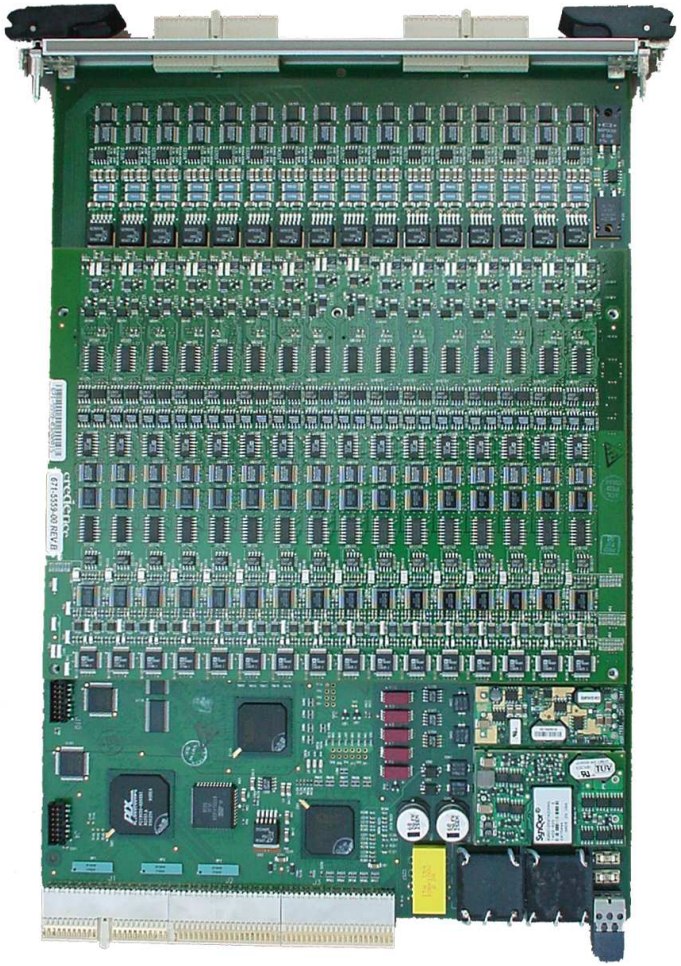
Pattern Execs (bursts & timing)

```
Pattern Easy {
EasyStart:
  W "wftEasy";
  V { all = 10; }
  V { all = 10 ; }
EasyStop:
  V { all = 01 ; }
Stop;
}
```

Patterns

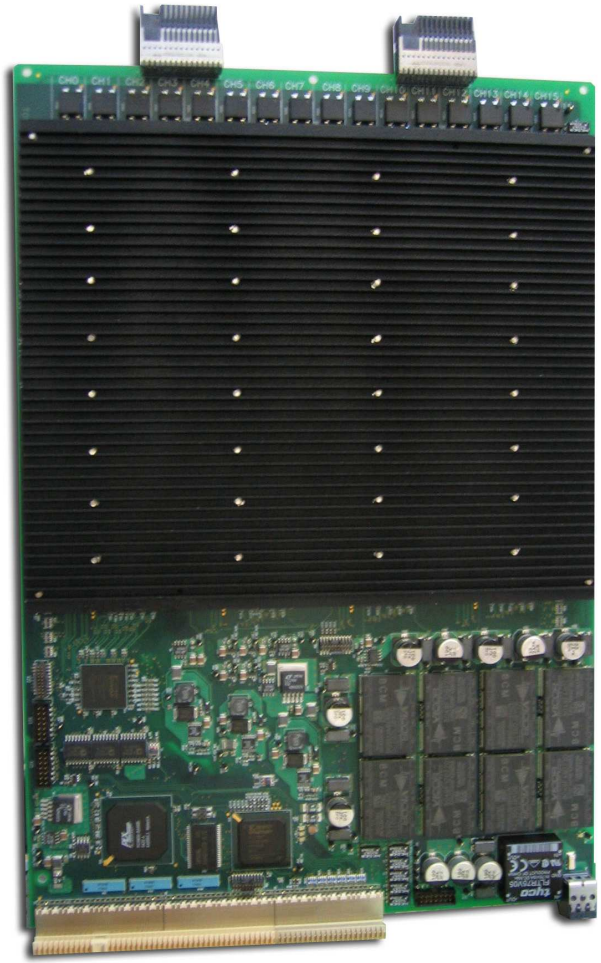
DPS16 Device Power Supply

- 16 source / measure channels
- Vforce:
  - 0 – 6 V positive only
  - 0.1% accuracy
  - 13 bit resolution
  - 2 amps per channel
  - 8 channels ganged to 16 amps
- Iranges:
  - 2A / 200mA / 2mA / 200uA
  - 0.2% accuracy
  - 16 bit resolution
- Current clamps:
  - 2% accuracy
  - 2A range
- Programmable / triggered 4k location cmd stack
- 64k location sample memory w/ on board averaging

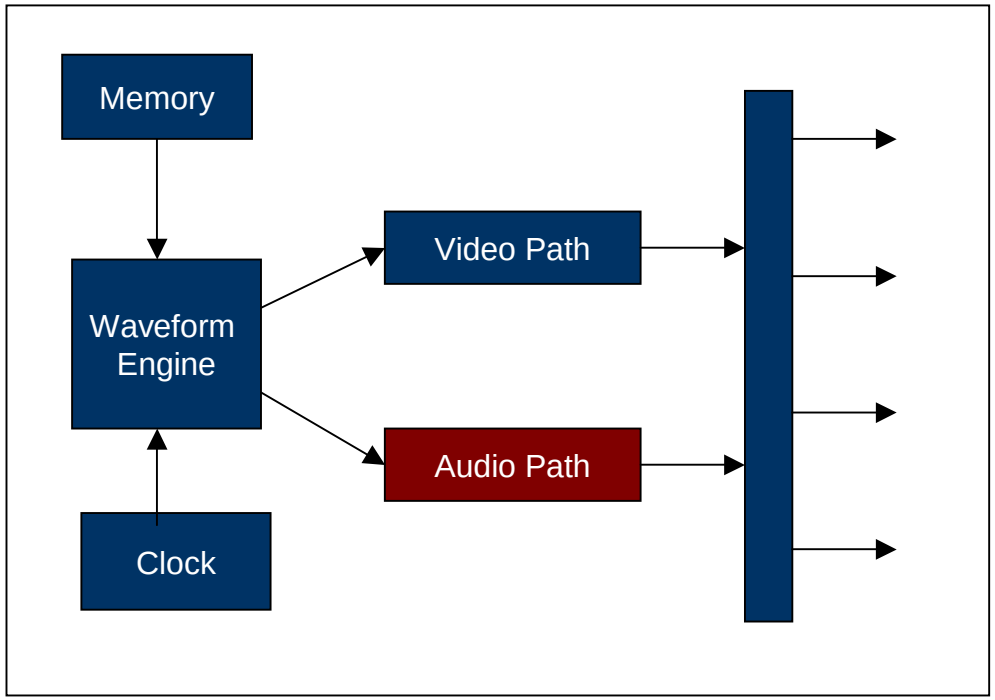


VIS16 – 4 Quadrant VI Source

- Sixteen VI source / measure channels
- Four quadrant operation in two configurations:
  - ±20V @ ±300mA
  - ±60V @ ±100mA
- 20V / 60V configuration programmable per channel
- Single ended voltage ranges:
  - ±2V / ±6V / ±20V / ±60V
- Differential voltage meas ranges (between 2 channels):
  - ±20mV / ±200mV / ±2V / ±10V
- Current ranges:
  - ±300nA / ±3uA / ±300uA / ±30mA / ±300mA
- ±.03% FSR accuracy / ±.01% FSR repeatability
- Programmable compensation for speed and stability
- Programmable low pass filter for measured functions
- Analog modulation up to 20kHz for PSRR tests
- Internal and external triggers for measurement sampling into 1024 location capture memory
- 50uF max capacitive load



D-10 AWG

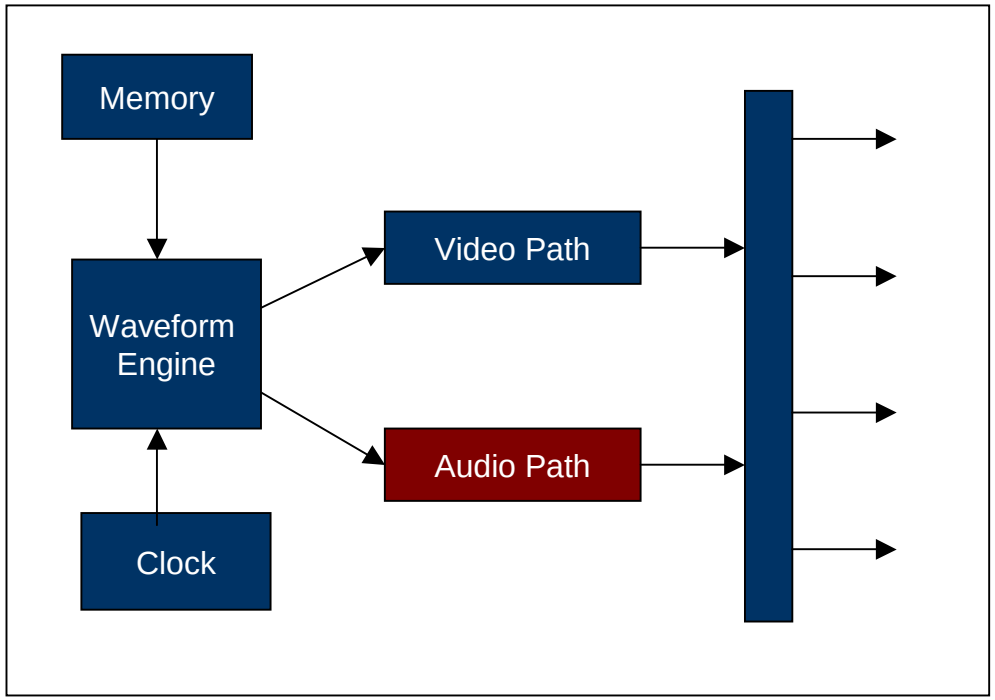


AWG

Multi-Site, Multi-Band AWG

- Channels can be used single-ended or differentially
- 4 channels share the same waveform memory and the same clocking
- Offset voltage is independently adjustable
- A high-frequency video path and a high-resolution audio path are available for each channel

D-10 AWG



AWG

Multi-Site AWG

- Sampling rate: 300Msps
- Audio w/1KHz BPF:
  - THD 120dB
  - SNR 105dB
- Video:
  - SNR 70dB
  - SFDR@20MHz 70dB

Instrument Clock

- Jitter < 3ps rms

Sapphire D-10 AWG

Feature	Sapphire D-10 AWG
Number of outputs	8 SE or 4 differential
Output impedance	50 Ohms
Output range (open circuit)	8V p-p with ±4V common offset and ±400mV independent offset
Hardware resolution	20 bits
Maximum sample rate	300 Msps
Waveform memory	1 Megaword
Bandwidth (3dB typical)	LF path: 2MHz, HF path: >100MHz

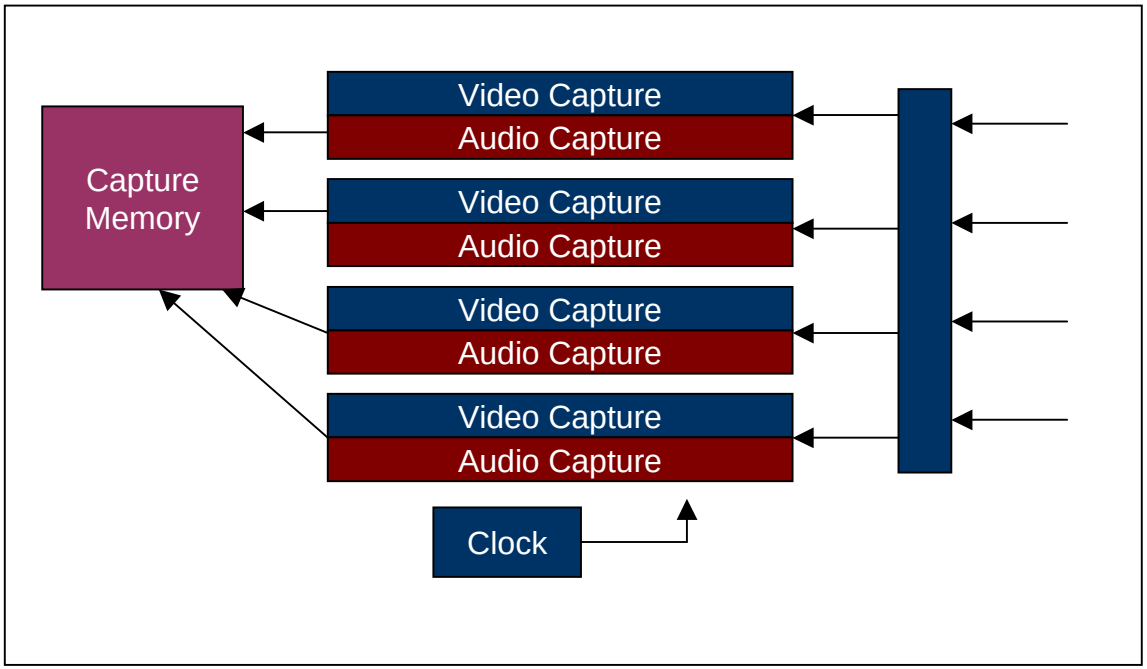
±

Sapphire D-10 AWG

Feature	Sapphire D-10 AWG
Jitter (typical)	3 ps rms
HF path filters	2 MHz, 6.3 MHz, 20 MHz, 63 MHz (LP, 5 pole Bessel)
LF path filters	2 kHz, 20 kHz, 200 kHz (LP, 6 pole Bessel) 1 kHz Bandpass (4^{th}-order Butterworth)
Noise density	8 $nV/Hz^{1/2}$ (HF path, 1V p-p into 50 Ohms)
SFDR (including harmonics)	85dB at 1MHz 70dB at 20MHz

±

D-10 Digitizer

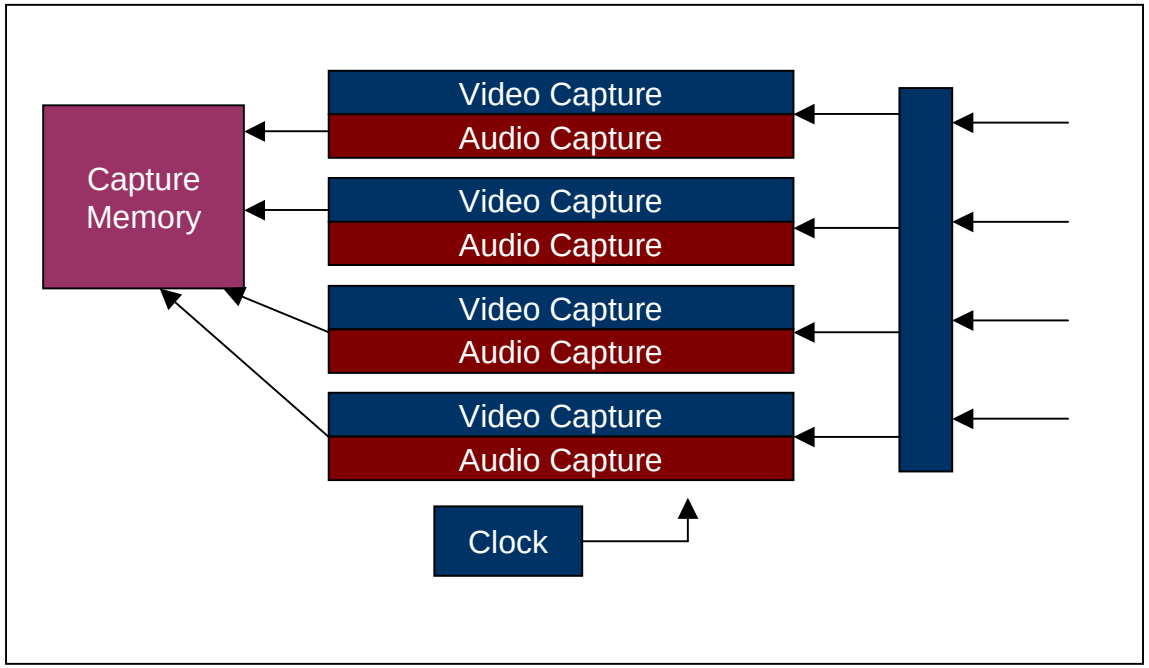


DIG

Multi-Site, Multi-band DIG

- 4 differential input channels share the same clocking and triggering
- A high-frequency video path and a high-resolution audio path are available for each channel

D-10 Digitizer



AVD

•Multi-Site DIG

- Sampling rate: 100Msps
- Audio w/1KHz notch:
  - THD 120dB
  - SNR 100dB
- Video
  - SNR 68dB
  - SFDR@20MHz 70dB

Instrument Clock

- Jitter < 3ps rms

Sapphire D-10 Digitizer

Feature	Sapphire D-10 DIG
Number of channels	4 differential
Input impedance	HF: 50 or 500 Ohms (100 or 1k Ohms differential) to Vterm, programmable from –2V to +6V LF: 10 Mohm or 600 Ohm
Input range	HF: 53mV to 4V (diff p-p, 2.5 dB steps) LF: 106 mV to 8 V (diff p-p, 2.5dB steps)
Maximum sample rate	100 Msps
Waveform memory	0.5 Megaword

Sapphire D-10 Digitizer

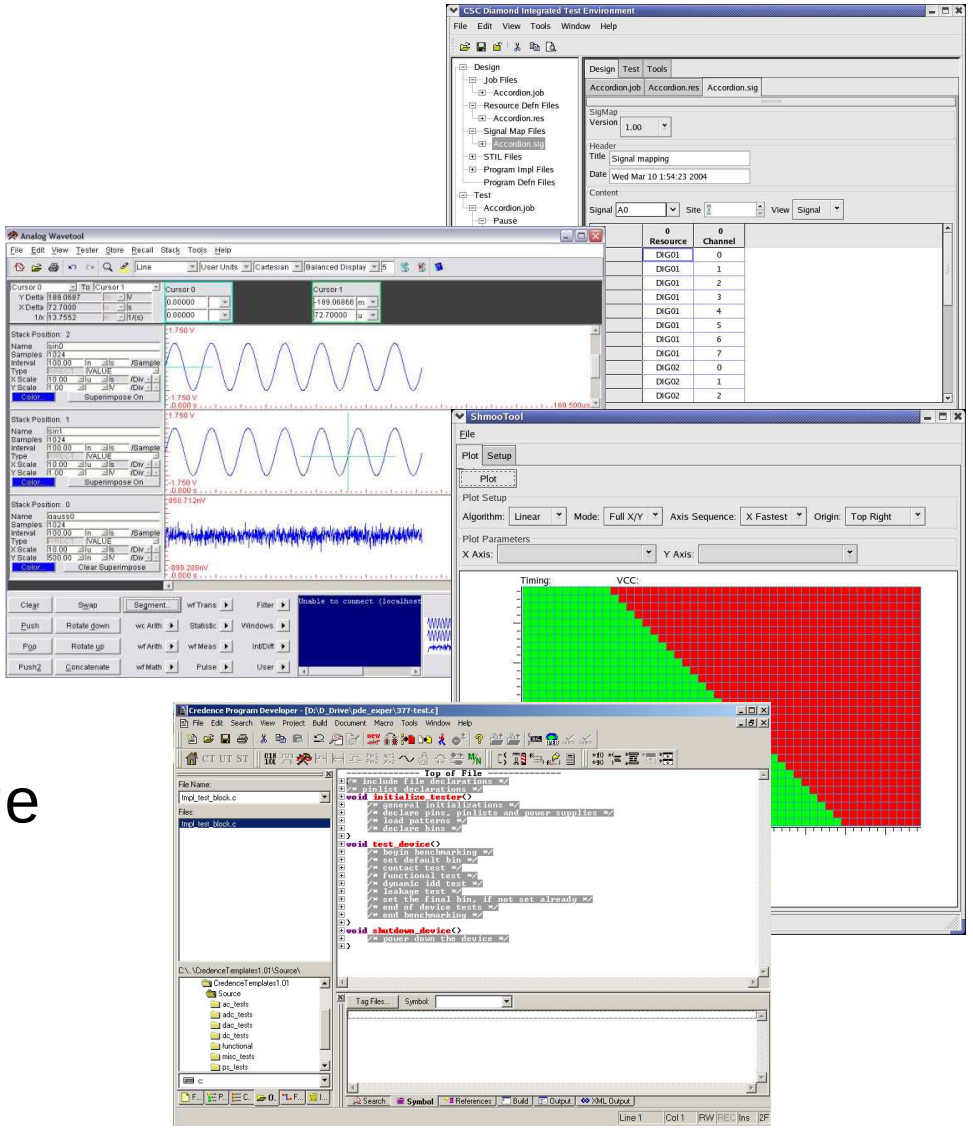
Feature	Sapphire D-10 DIG
ADC resolution	HF: 14 bits, LF: 16 bits
Bandwidth (3 dB typical)	HF: 230 MHz, LF: 4 MHz
Jitter (typical)	3 ps rms
Analog filters	HF: 20 MHz, 63 MHz (low pass, 5 pole Bessel) LF: 63 kHz, 250 kHz (low pass, 4 pole Bessel) 1 kHz (notch with 30 dB gain)
Halfband decimation filters	2x, 4x, 8x, 16x, 32x
Noise density	4 nV/Hz$^{1/2}$ (53 mV range) 22 nV/Hz$^{1/2}$ (4.0 V range)
SFDR (including harmonics)	70 dB at 20 MHz (SFDR is nearly flat below 20 MHz)

DIB Utility Board

- Always goes in slot 9 (last slot)
- Is required
- Fixed supplies
- Relay controls
- Communication busses

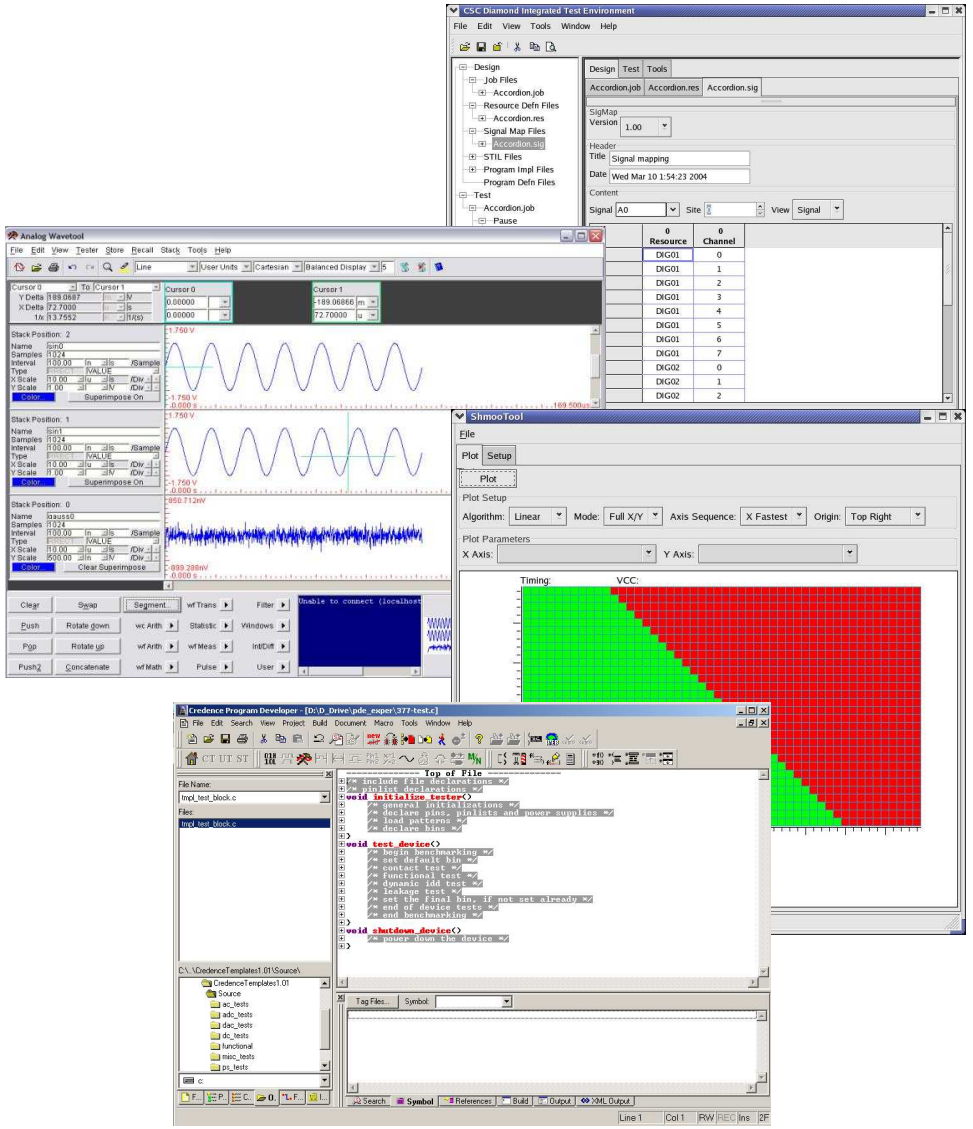
D-10 Software

- Simple
- Intuitive
- Open-architecture
- Fast response time
- Fast runtime
- Based on
  - Linux operating system
  - C++ test program language
  - STIL pattern format



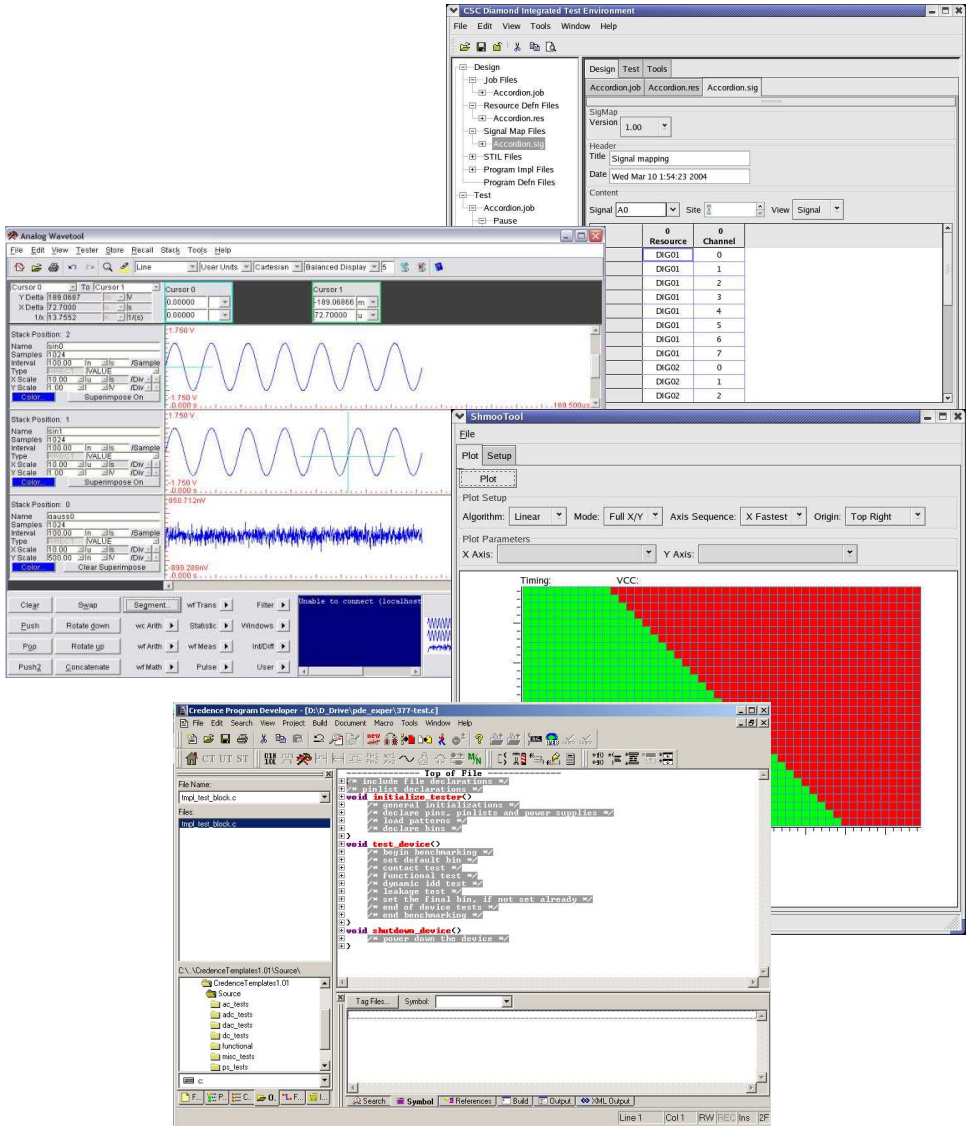
D-10 Software

- D-10 is committed to sharing interfaces, tools and formats with other Credence product lines as much as possible
  - STIL pattern format
  - Analog Wave Tool
  - Program Developer
  - Test Developer
  - Shmoo and Margin tool
  - Handler/prober interface
  - Galaxy data analysis
  - Datalogging formats
  - Test templates
  - Many more……

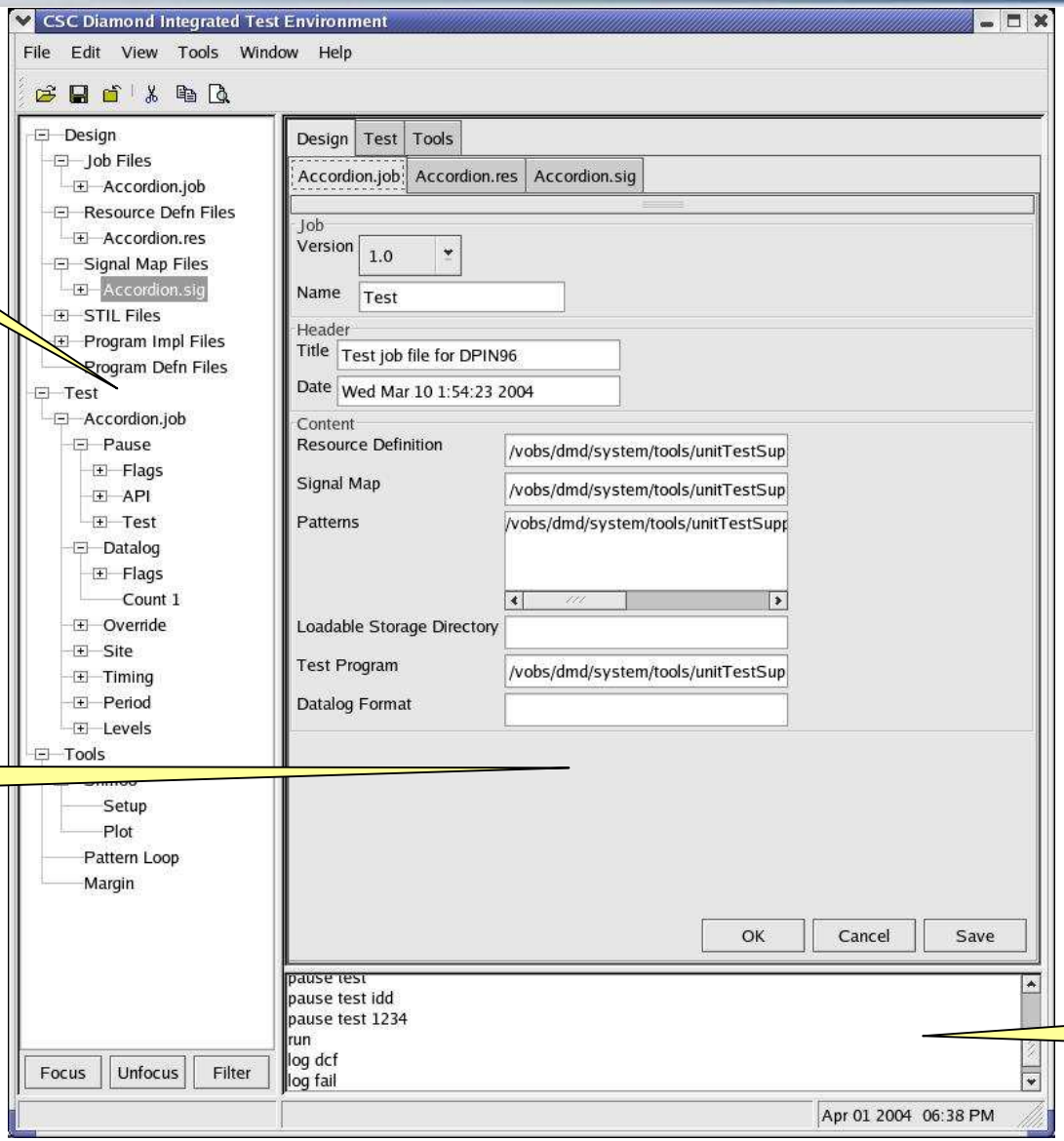


Integrated Test Environment (ITE)

- Project overview
  - Program files
  - Pattern files
  - Tester configuration details
- Operator interface
  - Test setup
  - Run control
  - Datalogging
- Interactive debugging tools
  - Shmoo and Margin tool
  - Pattern tool
  - Analog Wave Tool (AWT)
  - Pin and timing status displays
  - Program Developer tool
  - Interactive debug commands



Integrated Test Environment (ITE)



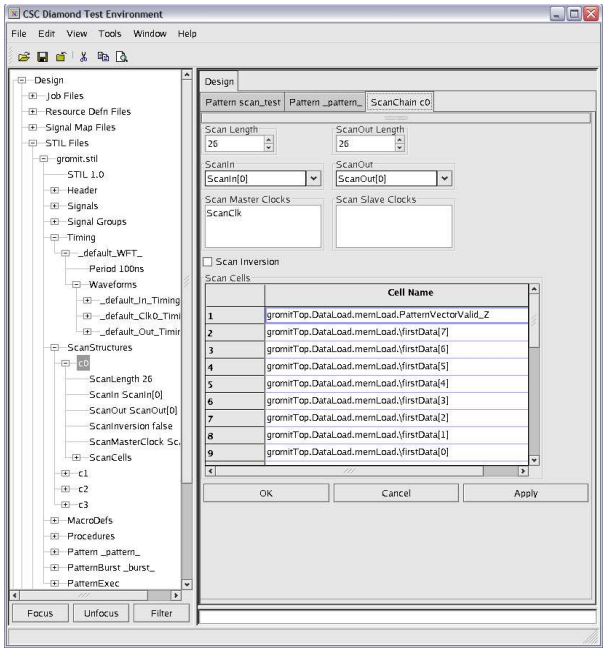
Navigation pane

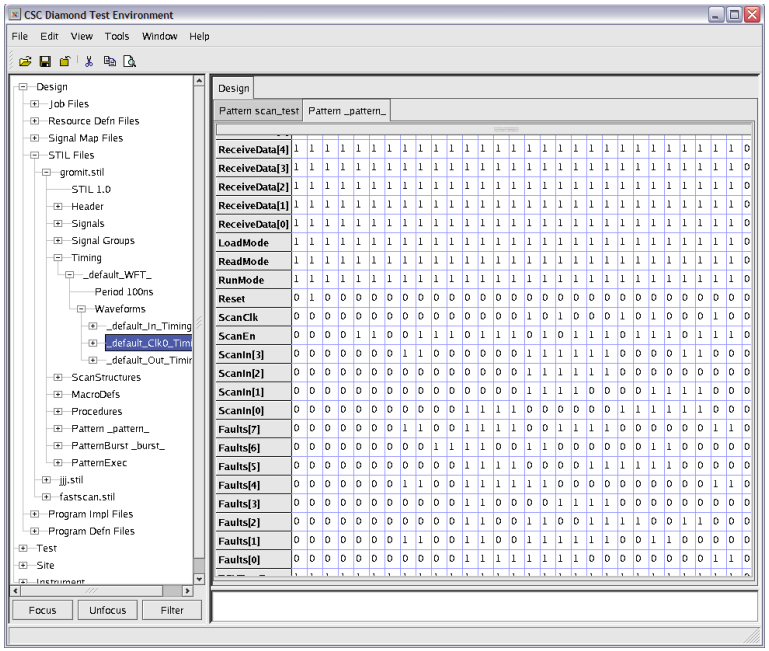
Display and Setup Pane

Output and Command Pane

Drag and drop entries from the navigation pane into the display pane to view, modify or launch the respective item

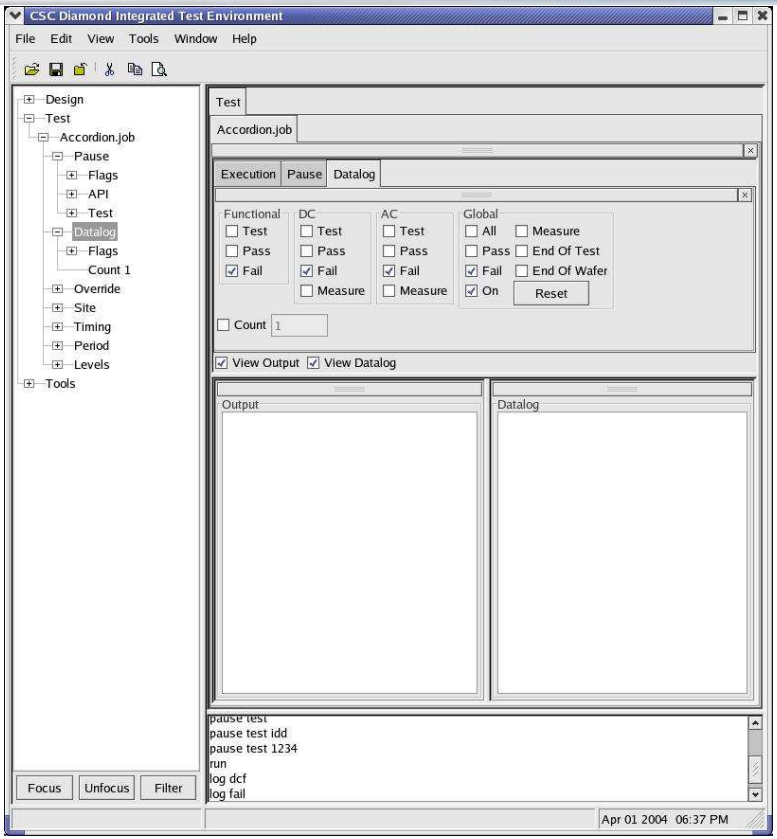
STIL in ITE



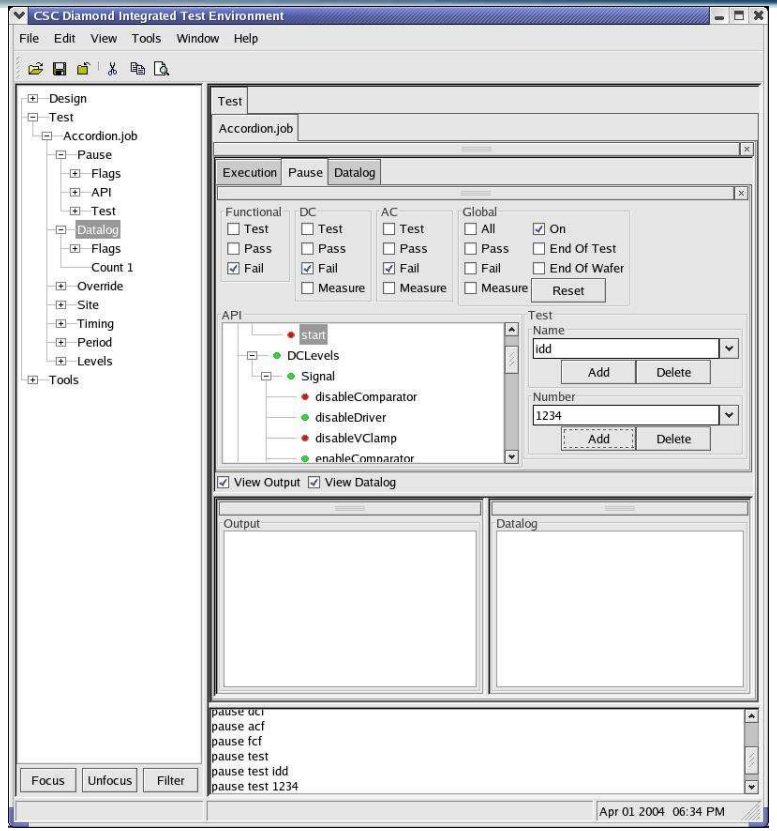


- Pattern, signal, pinlist and timing information is automatically extracted from the STIL file
- ITE provides a graphical display and edit interface for the STIL information

Control Panels



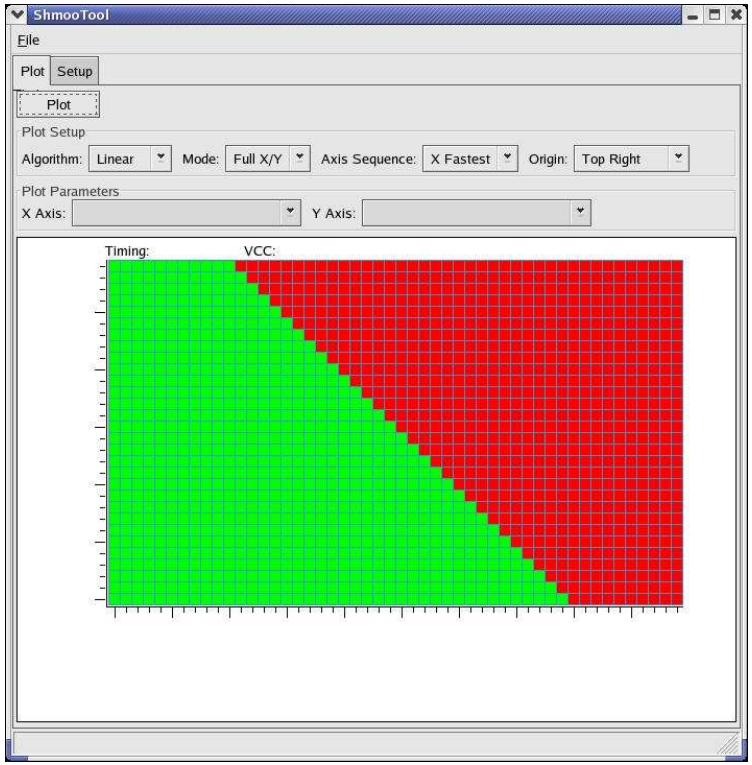
Datalogging



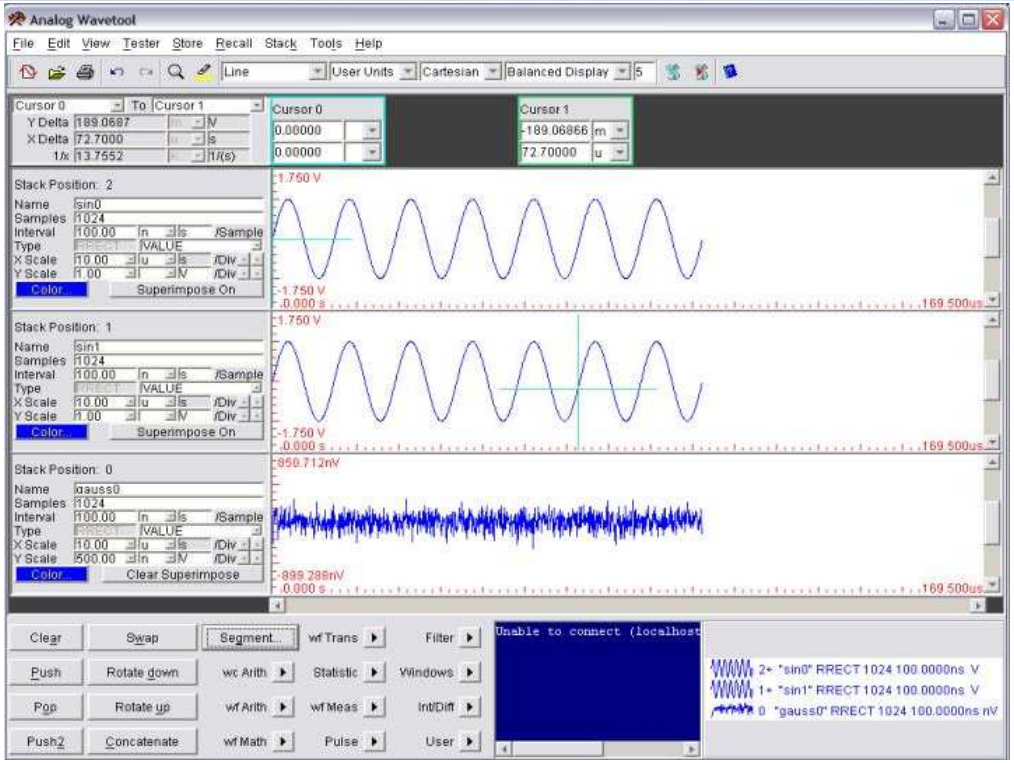
Pausing

- Simple control panels allow the user to control the program and set parameters such as pausing and datalogging flags

Debugging Tools



Shmoo & Margin



AWT

- Dragging and dropping tools into the display pane will cause them to launch with setups for the current breakpoint
- The display pane can be undocked

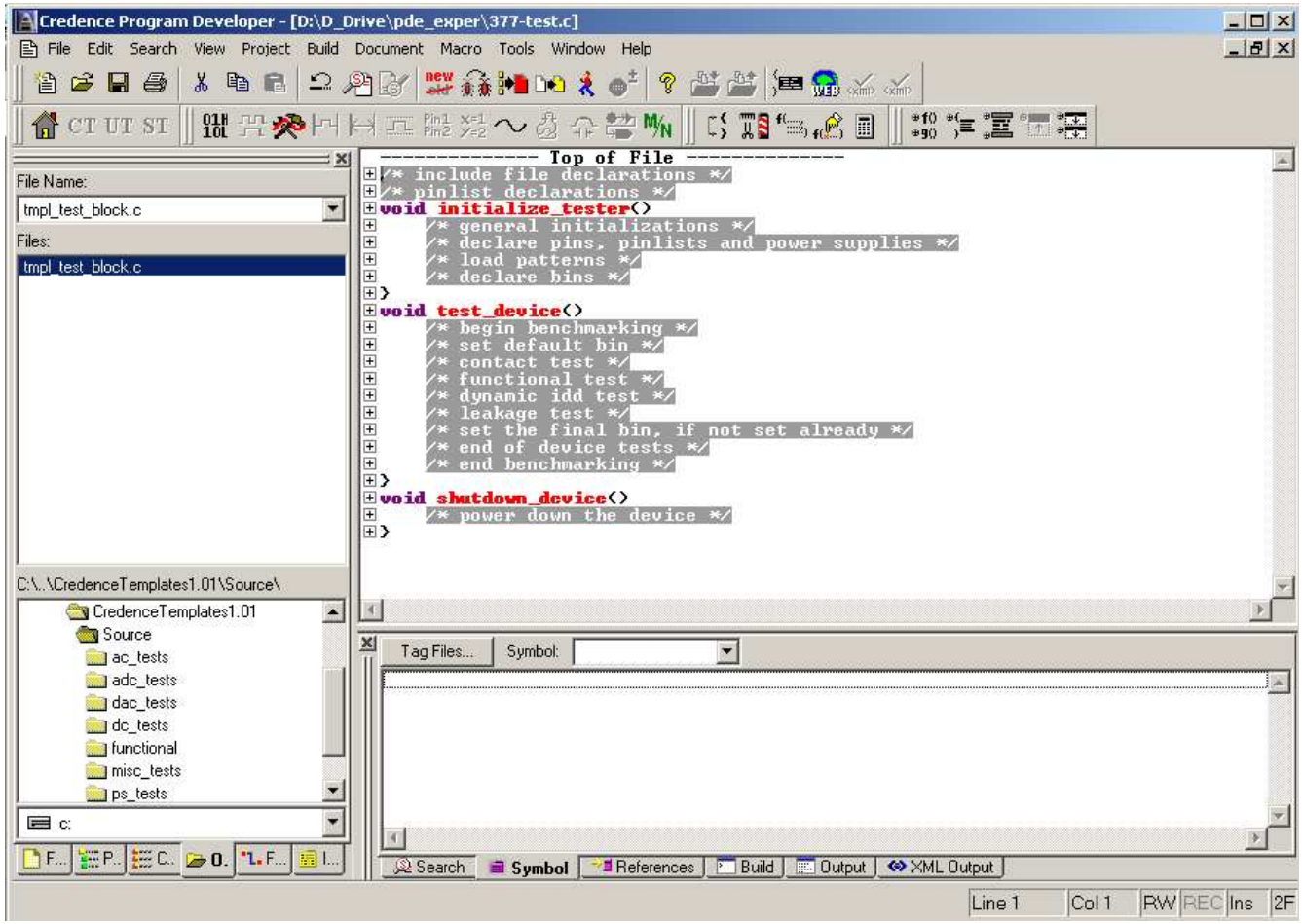
Credence Program Developer

- Available on D-10, Sapphire and Octet

- Powerful program development and debug environment based on the SlickEdit IDE

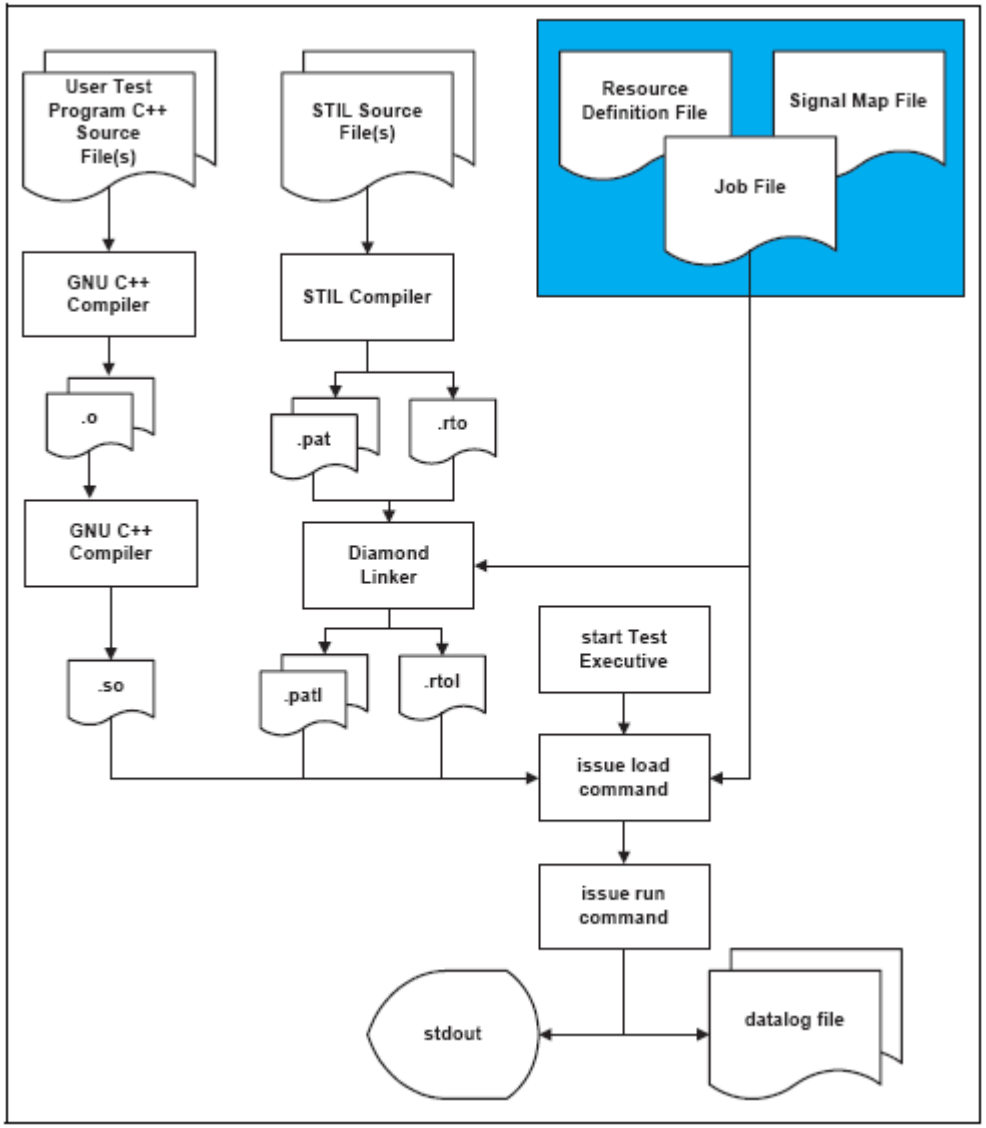
- Browser is used to navigate directories and organize test templates supplied by Credence or written by users

- Many standard IDE features such as
  - Source code debugger
  - Language-sensitive editor
  - Context-sensitive help
  - Much, much more…



- Program Developer is launched by ITE for test program development and debug

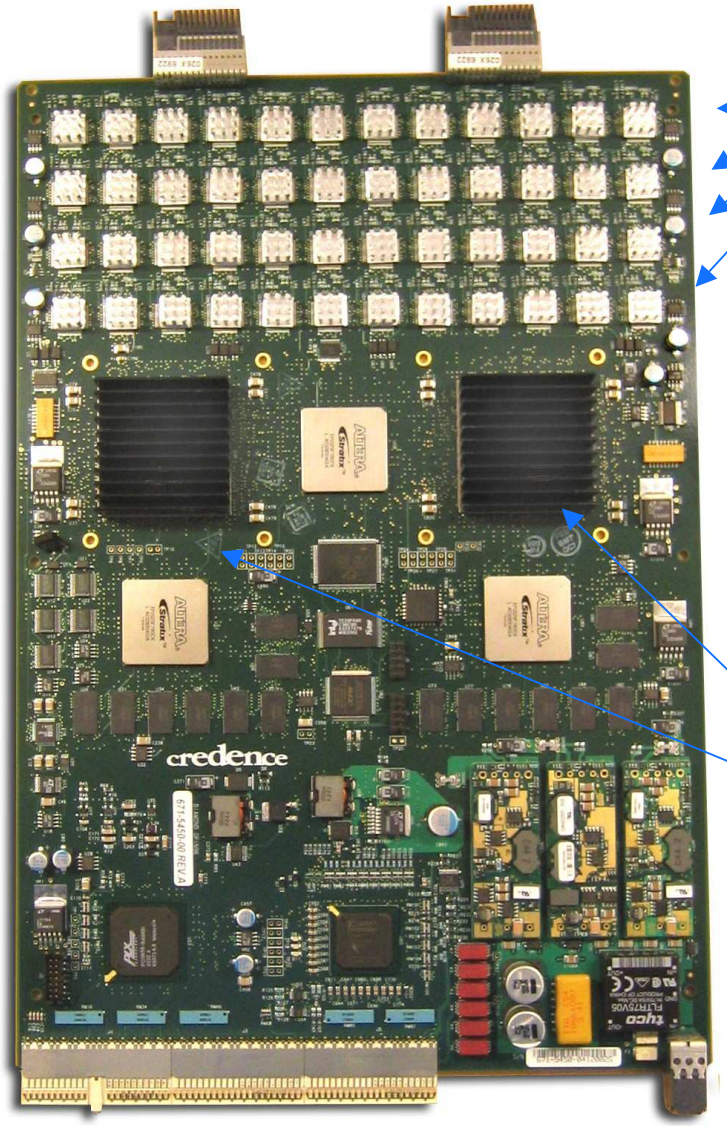
Source Files and Job Creation



Passive Load

credence

DPIN96

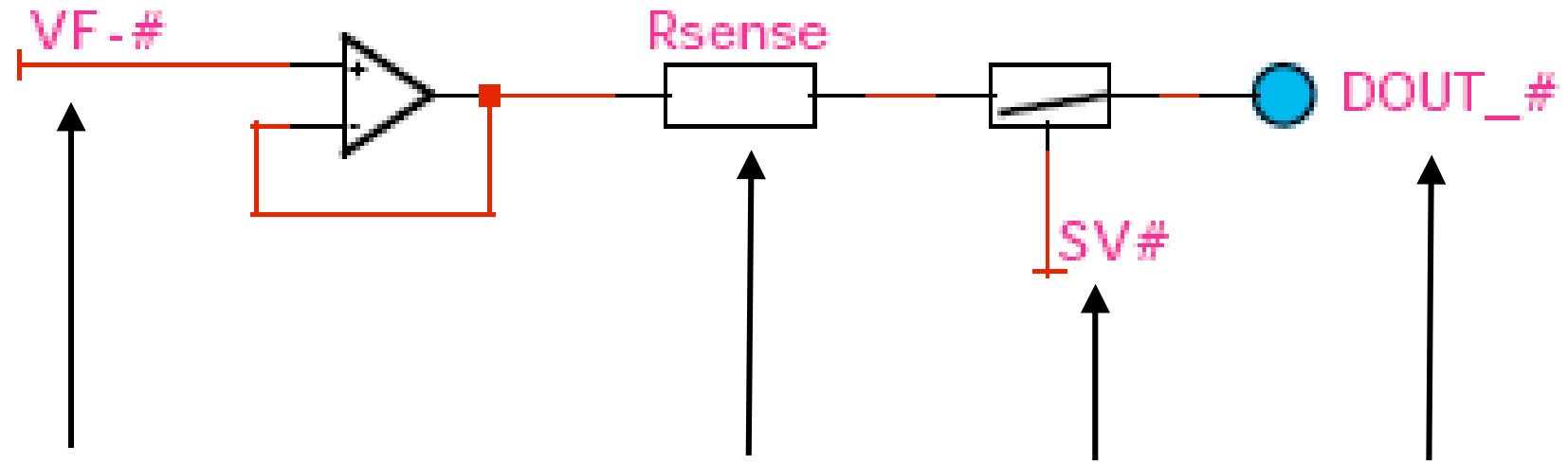


- PlanetATE driver/comparator/PMU dual channel devices
- Omni ASICS for timing and APG

DPIN96 Loads

- The DPIN96 has programmable loads per pin
- Loads consist of termination voltage connected through a resistive load
- The value of the resistive load is selected from a list of 8 possible values
- The termination voltage is programmable on a per-pin basis across the range of –1.5V to 12V
- Using the Ohm's Law, the proper values can be chosen to achieve the desired load current
- Both Ioh and Iol can be tested by running a 2-pass functional test with the loads set to the respective load currents for each pass

Static Load Circuit



PMU Force Voltage

Rsense
500 KΩ
125 KΩ
31.25 KΩ
7.81 KΩ
1.95 KΩ
500 Ω
125 Ω
31.25 Ω

Super Voltage

Connection to DUT Output

Force and Measure Current Ranges

Current Range	Imax	Rsense
IR0	2 µA	500 KΩ
IR1	8 µA	125 KΩ
IR2	32 µA	31.25 KΩ
IR3	128 µA	7.81 KΩ
IR4	512 µA	1.95 KΩ
IR5	2 mA	500 Ω
IR6	8 mA	125 Ω
IR7	32 mA	31.25 Ω