Testing Flash Memories

By Yi Gong

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CONTENTS

- Introduce to Flash Memory
- Faults in Memories
- Flash Memory Functional Test
- Flash Memory Parametric Test
- Flash Memory Reliability Test
Introduce to Flash Memory
What is Flash Memory?

- Flash Memory is an EEPROM
  - Electrical Programmable and Erasable
- Flash Memory is an NVM
  - Non-Volatile Memory
- Flash Cells can be erased simultaneously
  - Parallel Erasable
Introduce to Flash Memory

Flash Memory is Popular

2000 Memory Market

- DRAM: 78%
- NVM: 12%
- SRAM: 10%

2000 NVM Market

- Flash Memory: 55%
- ROM: 16%
- EPROM: 7%
- Other: 20%
Introduce to Flash Memory

Flash Memory Applications

- Wireless Applications
- Personal Digital Equipments
- Digital Set Top Boxes
- Automotive Applications
- Telecom and Networking Equipments
Introduce to Flash Memory

Flash Memory Market Share (2001)

Flash Memory Market Share 2001
(Webfeet Research)

- Intel 24%
- AMD 13%
- Sharp 10%
- Fujitsu 9%
- ST Micro 8%
- Toshiba 8%
- Mitsubishi 7%
- Atmel 4%
- Samsung 4%
- Others 13%

Testing Flash Memories
**Flash Memory Cell**

- **Gate**
- **Floating Gate**
- **Drain**
- **Source**

- **Program: Hot Electron Ejection**
- **Erase: Fowler-Nordheim Tunneling**
Introduction to Flash Memory

Floating Gate

The $V_t$ of a FGMOS transistor is given by:

- $V_t = K \cdot \frac{Q}{C_{ox}}$
- $K$: constant, depends on transistor properties
- $Q$: charge in FG
- $C_{ox}$: gate oxide capacitance

A: No Charge
B: Charged
Faults in Memories
Faults in Memories

Fault Manifestation

- Permanent Faults (hard faults)
  - Design faults
  - Broken components
  - Mask faults

- Non-Permanent Faults
  - Transient faults (caused by environment)
    - cosmic ray, alpha particles, temperature, pressure, humidity
  - Intermittent faults (not caused by environment)
    - Loose connection, aging components, noise
Faults in Memories

Failure Mechanisms

- Electrical Stress (in-circuit) Failure
  - Caused by poor design, ESD
- Intrinsic Failure Mechanisms
  - Crystal defects, process defects
- Extrinsic Failure Mechanisms
  - Metal deposition, bonding
Faults in Memories

Memory Fault Classification

- Functional Faults
  - Stuck at faults
  - Coupling faults
  - Pattern sensitive faults

- Parametric Faults
  - Leakage faults
  - Insufficient input/output level
  - Abnormal power consumption
Flash Memory
Functional Test
Flash Memory Functional Test

Reduced Flash Memory Functional Model

Address

Address Latch

Column Decoder

Row Decoder

Cell Array

Write Driver

Sense Amplifiers

Data Register

RE/WE/CE/OE

Blue: Address
Red: Data
Black: Control Signal

Data in/out

Testing Flash Memories
Functional Test Algorithms for Flash Memory

- Zero-One
- Checkerboard
- GALPAT
- Walking 1/0
- Sliding Diagonal
**Flash Memory Functional Test**

**Zero-One Algorithm**

- Also known as Memory Scan (MSCAN)

  - **Step 1:** Write 0 in all cells
  - **Step 2:** Read all cells
  - **Step 3:** Write 1 in all cells
  - **Step 4:** Read all cells

<table>
<thead>
<tr>
<th>All Cells</th>
<th>Step</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>W0</td>
</tr>
</tbody>
</table>

Testing Flash Memories 18
Flash Memory Functional Test

Test Coverage of Zero-One Algorithm

- Can’t detect all Address decoder faults.
- SAF will be detected as long as address decoder is correct.
- Not all Transient Faults are detected.
  - Cell may contain 0s before step 1.
- Not all coupling Faults are detected.
  - Cell may contain 0s before step 1.
Zero-One Algorithm (cont’d)

- Test length = $4 \times 2^N$ (N = Total Address Bits)
- Easy to implement
- Little test strength
Flash Memory Functional Test

**Checkerboard Algorithm**

- Cells are divided into two groups, cell-a and cell-b, forming a checkerboard pattern.
  - **Step 1:** Write 1 in all cell-a and 0 in cell-b
  - **Step 2:** Read all cells
  - **Step 3:** Write 0 in all cell-a and 1 in cell-b
  - **Step 4:** Read all cells

<table>
<thead>
<tr>
<th></th>
<th>a</th>
<th>b</th>
<th>a</th>
<th>b</th>
<th>a</th>
<th>b</th>
<th>a</th>
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<td></td>
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<td></td>
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</tbody>
</table>

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<th></th>
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<th>b</th>
<th>a</th>
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<th>b</th>
<th>a</th>
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<td>b</td>
<td>a</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Step</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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<tbody>
<tr>
<td>cell-a</td>
<td>w1</td>
<td>r1</td>
<td>w0</td>
<td>R0</td>
</tr>
<tr>
<td>cell-b</td>
<td>w0</td>
<td>r0</td>
<td>w1</td>
<td>r1</td>
</tr>
</tbody>
</table>
Flash Memory Functional Test

Test Coverage of Checkerboard Algorithm

- Not all Address Decoder faults are detected.
- SAF can be detected as long as the Address Decoder is correct.
- Not all Transient Faults are detected.
  - Initial cell status unknown.
- Not all Coupling Faults are detected.
  - Initial cell status unknown.
Flash Memory Functional Test

**Checkerboard Algorithm (Cont’d)**

- Detects shorts between adjacent cells
- Worse case test for leakage between adjacent cells
  - Each cell containing a 1 is surrounded by 0s
- Test length = $4 \times 2^N$ (N = Total Address Bits)
**GALPAT Algorithm**

- Memory is filled with 0s (or 1s) except for the base-cell, which contains a 1 (or 0). The base-cell walks through the whole array and all cells except the base-cell are read, after each other cell also the base-cell is read.
**Flash Memory Functional Test**

**GALPAT Algorithm (Cont’d)**

- **Step 1:** for \(d\) := 0 to 1 do
  
  begin
  
  for \(i\) := 0 to \(n-1\) do
  
  \(A(i) := d;\)

  for base-cell := 0 to \(n-1\) do
  
  begin
  
  \(A(base-cell) := d;\)

  Goto READ

  \(A(base-cell) := d;\)

  end;

  end;

- **Step 2:**
  
  \(A(base-cell) := d;\)

  Goto READ

  \(A(base-cell) := d;\)

  end;

- **Step 3:**
  
  {READ}

  begin
  
  for cell := 0 to \(n-1\) do
  
  begin
  
  if \((A(cell) <> d)\) then output (“Error at cell”, cell);

  if \((A(base-cell) <> d)\) then output (“Error at cell”, cell);

  end

  end
Flash Memory Functional Test

Test Coverage of GALPAT Algorithm

- All Address Decoder Faults are detected and located.
- All SAF will be located because the base-cell is written and read with 0 and 1.
- All Transient Faults are located because the base-cell make transitions after which it is read.
GALPAT Algorithm (Cont’d)

- Test length = $2^N + 2^n + 2n^2$
  - $N =$ Total Address Bits
  - $n =$ Total Cell Number

- Capable of locating all Address Decoder Faults and Coupling Faults.
**Walking 1/0 Algorithm**

Memory is filled with 0s (or 1s) except for the base-cell, which contains a 1 (or 0). The base-cell walks through the whole array and all cells except the base-cell are read, after all other cells also the base-cell is read.
Flash Memory Functional Test

Walking 1/0 Algorithm (Cont’d)

- **Step 1:** for \( d := 0 \) to 1 do
  
  begin
  
  for \( i := 0 \) to \( n - 1 \) do
  
  \( A(i) := d; \)
  
  for base-cell := 0 to \( n - 1 \) do
  
  begin
  
  end
  
  end

- **Step 2:**
  
  \( A(\text{base-cell}) := d'; \)
  
  Goto READ
  
  \( A(\text{base-cell}) := d; \)
  
  end;

- **Step 3:**
  
  \{READ\}
  
  begin
  
  for cell := 0 to \( n - 1 \) do
  
  begin
  
  if \( A(\text{cell}) <> d \) then output (“Error at cell”, cell);
  
  end;

  if \( A(\text{base-cell}) <> d' \) then output (“Error at cell”, cell);

  end
**Test Coverage of Walking 1/0 Algorithm**

- All Address Decoder Faults are detected and located.
- All SAF will be located because the base-cell is written and read with 0 and 1.
- All Transient Faults are located because the base-cell makes transitions after which it is read.
Walking 1/0 Algorithm (Cont’d)

- Test length = $2 \times (2^N + 2 \times n + n^2)$
  - $N =$ Total Address Bits
  - $n =$ Total Cell Number
- Capable of locating all Address Decoder Faults and Coupling Faults.
Sliding Diagonal Algorithm

- Designed as a shorter alternative to GALPAT, it uses a diagonal of base cells instead of a single base cell.
- Cells on the diagonal are used because each cell has a different row and column address, simultaneously checking the row and column decoder.
- The algorithm writes a diagonal of 1s to a background of 0s. All cells are read, after which the diagonal is shifted.
Sliding Diagonal Algorithm (Cont’d)

- Repeat the process until every cells are on the diagonal.
- The whole sequence is then done again with inverted data.
Sliding Diagonal Algorithm (Cont’d)

For \( d := 0 \) to 1 do

Begin

Write \( d \) to all non-diagonal cells;

Write \( d' \) to all diagonal cells;

For \( \text{diag} := 0 \) to \( \text{maxcolumn-1} \) do

Begin

\{READ: read all cells\}

for \( i := 0 \) to \( \text{maxrow-1} \) do

begin

\( A(i, \text{diag}+i) := d' \);

\( A(i, \text{diag}+i+1) := d \);

end.

end;

end;
Test Coverage of Sliding Diagonal Algorithm

- Not all Address Decoder Faults will be detected since faults on cells on the same diagonal may mask each other.
- All SAF and Transient Faults are detected and located, since every cell is written when it becomes part of the diagonal followed by read action. Both transitions occur with inverted data.
- Not all Coupling Faults will be detected, because all diagonal cells are written consecutively.
**Sliding Diagonal Algorithm (Cont’d)**

- Test length $= 2 \times (n + n^{1/2} \times (n + 2n^{1/2}))$
  - $n =$ Total Cell Number
- Less test coverage compared with GALPAT
- More efficient
Flash Memory

Parametric Test
Flash Memory Parametric Test

Purpose of Parametric Test

- Characterization Test:
  - To determine the exact value of a DC or AC parameter at which a device fails.

- Go/NoGo Test (Production Test)
  - To determine whether a device meets its specifications.
Flash Memory Parametric Test

Classification of Parametric Test

- DC Parametric Test
  - Contact test
  - Power consumption test
  - Leakage test
  - Threshold test
  - Output drive current test
  - Output short current test
Classification of Parametric Test

- AC Parametric Test
  - Test for rise and fall times
  - Test for setup and hold times
  - Test for measuring delay times
  - Test for access time
  - Speed tests
Contact Test

To ensure that the tester is in contact with the device, also checks for opens and shorts of the device pins. Done as the first test.
Contact Test (Cont’d)

- Set all pins to 0V
- Force a forward biasing current $I_b$ through the diodes; typical value: $100\mu A \leq I_b \leq 250\mu A$.
- Measure the voltage $V_b$ at the pin:
  - $V_b < 0.1V$ (short)
  - $0.1V \leq V_b \leq 1.5V$ (normal)
  - $V_b > 1.5V$ (open)
Power Consumption Test

- Measuring the maximum current through the device while the power supply voltage \( V_{in} \) is at its specified value.
  - Static Power Consumption Test
    - To determine the worst-case power consumption while the inputs have a steady logical value.
  - Dynamic Power Consumption Test
    - To measure the worst-case power consumption while the device is operational.
**Leakage Test**

- CMOS inputs and tristated outputs should be considered as open circuits; in reality both appear as a high impedance. The amount of worst-case current drawn is called leakage.
  - Input Leakage
  - Tristate Leakage
Flash Memory Parametric Test (DC)

**Leakage Test**

- **Input Leakage Test:**
  - Force input pin a voltage and measure the current

- **Tristate Leakage Test:**
  - Measure the tristated output with PMU.
**Threshold Test**

- Determine the maximum input voltage at which the device will switch from high to low. ($V_{IL}$)
- Determine the minimum input voltage at which the device will switch from low to high. ($V_{IH}$)

![Switching Area Diagram]

- Logic 0
- Switching Area
- Logic 1

- $0V$
- $V_{IL}$
- $V_{IH}$
- $V_{CC}$
**Output Drive Current Test**

- The purpose is to ensure the device can hold its specified output voltage level while driving the specified current.
- This test is done by forcing the output voltage and measure the current.
Output Short Current Test

- The purpose is to verify the drive capability of the output drivers.
- Set output pin to 1, the output voltage of the PMU is forced to 0V and measure the output current.
Introduction to AC Parametric Test

- Timing measurement.
- The purpose is to ensure the changes in output values occur at the right time.
Classification of AC Parametric Test

- **Rise and fall time measurement:**
  - Check the speed with which an output signal can change state.

- **Setup and hold time measurement:**
  - Tests for race conditions between input signals.

- **Delay time measurement:**
  - Tests for the delay time between the input stimulus and output response.

- **Speed measurement:**
  - Measure the time interval between the application of input stimuli and their response. Test the speed of the device.
Test for Rise and Fall Times

Rise Time  Fall Time

VOH  VOH
VOL  VOL
Tests for Setup and Hold Times

- **Setup time:**
  - The amount of time the input data is required to be present before the edge of the control input occurs.

- **Hold time:**
  - The amount of time the input data has to remain valid after the edge of the control input has occurred.
Tests for Setup and Hold Times (Cont’d)
Tests for Delay Times

- Measures the length of the time interval between input and the output.

- $T_{PHL}$:
  - Propagation delay from the 50% of the input voltage until the output low voltage $V_{OL}$.

- $T_{PLH}$:
  - Propagation delay from the 50% of the input voltage until the output high voltage $V_{OH}$. 
Tests for Delay Times (Cont’d)

- **Input 50% Point**
- **Output V_{OL}**
- **Input 50% Point**
- **Output V_{OH}**

**T_{PHL}**

**T_{PLH}**
Tests for Access Times

- Assume the memory is functionally correct.
- $T_A$ is defined as the longest of the two delay times between the 50% point of the voltage on the address lines and the H/L points of data outputs.
Tests for Access Times (Cont’d)
**Speed Tests**

- Assume the memory is functionally correct.
- Measure the read/write time of memory locations.
A Schmoo plot is used to visualize the inter-dependence of the two variables.

Used to identify safety margins, frequently used in parametric tests.
Typical Read Timing Specification

(AMD Am29F010B)

Read-only Operations Characteristics

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Parameter Description</th>
<th>Test Setup</th>
<th>Speed Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{RCC}$</td>
<td>Read Cycle Time (Note 1)</td>
<td>$t_{ACC}$</td>
<td>$t_{OEH}$, $t_{OE}$, $t_{OH}$</td>
</tr>
<tr>
<td>$t_{AV}$</td>
<td>Address to Output Delay</td>
<td>$OE, OE = VIL$</td>
<td>Max</td>
</tr>
<tr>
<td>$t_{QOV}$</td>
<td>Chip Enable to Output Delay</td>
<td>$OE, OE = VIL$</td>
<td>Max</td>
</tr>
<tr>
<td>$t_{QOV}$</td>
<td>Output Enable to Output Delay</td>
<td>Max</td>
<td>25 30 30 35 50 ns</td>
</tr>
<tr>
<td>$t_{DHZ}$</td>
<td>Chip Enable to Output High Z (Note 1)</td>
<td>Max</td>
<td>10 15 20 20 30 ns</td>
</tr>
<tr>
<td>$t_{OHZ}$</td>
<td>Output Enable to Output High Z (Note 1)</td>
<td>Max</td>
<td>10 15 20 20 30 ns</td>
</tr>
<tr>
<td>$t_{OEH}$</td>
<td>Output Enable Hold Time (Note 1)</td>
<td>Read</td>
<td>Min</td>
</tr>
<tr>
<td>$t_{QOH}$</td>
<td>Output Hold Time From Addresses CE or OE, Whichever Occurs First</td>
<td>Min</td>
<td>10 ns</td>
</tr>
<tr>
<td>$t_{AVX}$</td>
<td></td>
<td></td>
<td>Min</td>
</tr>
</tbody>
</table>
**Typical Program Timing Specification**

(AMD Am29F010B)

### Erase and Program Operations

<table>
<thead>
<tr>
<th>Parameter Symbol</th>
<th>Parameter Description</th>
<th>JEDEC Std</th>
<th>Parameter Description</th>
<th>Speed Options</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{WAC}</td>
<td>Write Cycle Time (Note 1)</td>
<td>Min</td>
<td>t_{WAC}</td>
<td>45 55 70 90 120</td>
<td>ns</td>
</tr>
<tr>
<td>t_{AS}</td>
<td>Address Setup Time</td>
<td>Min</td>
<td>t_{AS}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{AH}</td>
<td>Address Hold Time</td>
<td>Min</td>
<td>t_{AH}</td>
<td>35 45 45 45 50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{DS}</td>
<td>Data Setup Time</td>
<td>Min</td>
<td>t_{DS}</td>
<td>20 30 45 50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{DH}</td>
<td>Data Hold Time</td>
<td>Min</td>
<td>t_{DH}</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>t_{OES}</td>
<td>Output Enable Setup Time</td>
<td>Min</td>
<td>t_{OES}</td>
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<tr>
<td>t_{RBL}</td>
<td>Read Recover Time Before Write (CE# High to WE# Low)</td>
<td>Min</td>
<td>t_{RBL}</td>
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<tr>
<td>t_{CS}</td>
<td>CE# Setup Time</td>
<td>Min</td>
<td>t_{CS}</td>
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<tr>
<td>t_{CH}</td>
<td>CE# Hold Time</td>
<td>Min</td>
<td>t_{CH}</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>t_{WP}</td>
<td>Write Pulse Width</td>
<td>Min</td>
<td>t_{WP}</td>
<td>25 30 35 45 50</td>
<td>ns</td>
</tr>
<tr>
<td>t_{WPH}</td>
<td>Write Pulse Width High</td>
<td>Min</td>
<td>t_{WPH}</td>
<td>20</td>
<td>ns</td>
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<tr>
<td>t_{PH1}</td>
<td>Byte Programming Operation (Note 2)</td>
<td>Typ</td>
<td>t_{PH1}</td>
<td>7</td>
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</tr>
<tr>
<td>t_{PH2}</td>
<td>Chip/sector Erase Operation (Note 2)</td>
<td>Typ</td>
<td>t_{PH2}</td>
<td>1.0</td>
<td>sec</td>
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<tr>
<td>t_{VCS}</td>
<td>V_{CC} Set Up Time (Note 1)</td>
<td>Min</td>
<td>t_{VCS}</td>
<td>50</td>
<td>μs</td>
</tr>
</tbody>
</table>

![Program Command Sequence](image1)

![Read Status Data](image2)
Flash Memory

Reliability Test
Production Test Hierarchy

- Production Test
  - Wafer Level Test
    - Wafer Electrical Test
    - Circuit Probe
  - Reliability Test
    - Temp Acceleration
    - Current/Voltage Accelerate
  - Final Test
    - Initial Class test
    - Quality Assurance
    - Temp Cycle
    - Burn-in
Flash Memory Reliability Test

Production Test Flow

- Wafer Test
- Package Test (Final Test)
- Quality Assurance
- Reliability Test
Flash Memory Reliability Test

Reliability Test Purposes

- To ensure that the circuit will perform its stated functions under given operating conditions for at least a specific period of lifetime.

- The screening process selects chips with superior reliability and rejects those which potentially will fail early during operation.
**Reliability and Failure Rate**

- Reliability of a system may be stated in terms of system failure rate or Mean Time Between Failures.
- **MTBF** (Mean Time Between Failures)
  - For a constant failure rate
    \[ MTBF = \frac{1}{R} \] (R is the failure rate)
- **FIT** (Failure Unit)
  - Failure per unit time
    \[ 1 \text{ FIT} = \text{one failure in } 10^9 \text{ device hours} \]
Flash Memory Reliability Test

Reliability and Failure Rate (Cont’d)

Infant Mortality

Normal Life

Wear-Out

<Failure Rate>

<Time>

Burn-In

1K Hours

10-25 Years

 Depends on the maturity of the manufacturing and packaging processes

Testing Flash Memories
Reliability Failure Mechanisms

- Chip Related Failures
  - Dopant diffusion
  - Ionic movement
  - Oxide contamination
  - Dielectric breakdown
  - Metal voiding
  - Metal interconnect cracking
Flash Memory Reliability Test

Reliability Failure Mechanisms (Cont’d)

- Assembly Related Failures
  - Mounting voids
  - Thermal mismatching
  - Metal stress relaxation
  - Oxidation
Reliability Failure Mechanisms (Cont’d)

- Operation Induced Failures
  - Electromigration
  - Hot carriers
  - Electrostatic discharge
Flash Memory Reliability Test

Reliability Test Classification

- Pressure Cooker Test (PCT)
- Temperature Cycle Test (TCT)
- Thermal Shock Test (TST)
- Temperature, Humidity Bias Test (THB)
- Highly Accelerated Stress Test (HAST)
- High Temperature Operating Life Test (HTOL)
- Low Temperature Operating Life Test (LTOL)
- High Temperature Storage (HTS)
Flash Memory Reliability Test

**Pressure Cooker Test**

- To assess the ability of a product to withstand severe temperature and humidity conditions.

- **Test Conditions:**
  - Soaking the samples for 168 hours at 121 deg C, 100% RH, and 2 atm.
Flash Memory Reliability Test

Temperature Cycle Test

- Determine the ability of samples resist extremely low and high temperatures and their ability to withstand cyclical exposures to there conditions.

- Test Conditions:

**Mil Std 883, Method 1010 Specs:**
- Must be conducted for a minimum of 10 cycles
- Condition A: -55 (+0/-10) deg C to 85 (+10,-0) deg C
- Condition B: -55 (+0/-10) deg C to 125 (+15,-0) deg C
- Condition C: -65 (+0/-10) deg C to 150 (+15,-0) deg C
- Condition D: -65 (+0/-10) deg C to 200 (+15,-0) deg C
- Condition E: -65 (+0/-10) deg C to 300 (+15,-0) deg C
- Condition F: -65 (+0/-10) deg C to 175 (+15,-0) deg C
- Total Transfer Time <= 1 minute
- Total Dwell Time >= 10 minutes
- Specified Temp reached in <= 15 minutes

**JEDEC JESD22-A104-A Specs:**
- Recommended for lot acceptance screen: 10 cycles
- Recommended for qualification: 1000 cycles
- Condition A: -55 (+0/-10) deg C to 85 (+10,-0) deg C
- Condition B: -55 (+0/-10) deg C to 125 (+10,-0) deg C
- Condition C: -65 (+0/-10) deg C to 150 (+10,-0) deg C
- Condition D: -65 (+0/-10) deg C to 200 (+10,-0) deg C
- Condition F: -65 (+0/-10) deg C to 175 (+10,-0) deg C
- Condition G: -40 (+0/-10) deg C to 125 (+10,-0) deg C
- Condition H: -55 (+0/-10) deg C to 150 (+10,-0) deg C
- Total Transfer Time <= 1 minute
- Total Dwell Time >= 10 minutes
- Specified Temp reached in <= 15 minutes
Flash Memory Reliability Test

Thermal Shock Test

- Determine the resistance of the part to sudden changes in temperature.
  - The parts undergo a specified number of cycles, which start at ambient temperature.
  - Then expose the parts to an extremely low temperature.
  - After a short while, the parts are exposed to an extremely high temperature.
Thermal Shock Test (Cont’d)

Test Conditions:

**Mil Std 883, Method 1011 Specs:**
- Must be conducted for a minimum of 15 cycles
- Condition A: 0 (+2/-10) deg C to 100 (+10/-2) deg C
- Condition B: -55 (+0/-10) deg C to 125 (+10,0) deg C
- Condition C: -65 (+0/-10) deg C to 150 (+10,0) deg C
- Total Transfer Time < 10 seconds
- Total Dwell Time > 2 minutes
- Specified Temp reached in < 5 minutes

**JEDEC JESD22-A106-A Specs:**
- Must be conducted for a minimum of 15 cycles
- Condition A: -40 (+0/-30) deg C to 85 (+10/-0) deg C
- Condition B: -0 (+2/-10) deg C to 100 (+10,-2) deg C
- Condition C: -55 (+0,-10) deg C to 125 (+10,-0) deg C
- Condition D: -65 (+0,-10) deg C to 150 (+10,-0) deg C
- Total Transfer Time < 10 seconds
- Total Dwell Time > 2 minutes
- Specified Temp reached in < 5 minutes
Flash Memory Reliability Test

Temperature, Humidity, Bias Test

- To accelerate metal corrosion, particularly that of the metallization on the die surface.

- Test Conditions:
  - 1000 hours at 85 deg C, 85% RH, with bias applied to the device.
Flash Memory Reliability Test

Highly Accelerated Temperature Stress Test

- To shorten the THB test.
- Take 96-100 hours.
- Test Conditions:
  - 130 deg C and 85% RH with bias for 96-100 hours.
Highly Accelerated Operating Life Test

Determine the reliability of devices under operation at high temperature conditions over an extended period of time.

Concerned with wear-out failures.

Test Conditions:

**Mill Std 883, Method 1005 Specs:**
- generally 1000 hours min. at 125 deg C
- max. rated Tc or Ta < 200 deg C (Class B)
- max. rated Tc or Ta < 175 deg C (Class S)
- Condition A: steady-state, reverse bias
- Condition B: steady-state, forward bias
- Condition C: steady-state, power/reverse bias
- Condition D: steady-state, parallel excitation
- Condition E: steady-state, ring oscillator
- Condition F: steady-state, temp.-accelerated

**Other HTOL Conditions (depending on use):**
- \( Ta=125C, 1000H, \) max Pdis
- \( Ta=150C, 500H, \) max Pdis
- \( 125C<Tj<150C, 1000H, \) max Pdis
- \( 150<Tj<175C, 500H, \) max Pdis
- \( Ta=125C, 1000H, \) Dyn, max Pdis
- \( Ta=150C, 500 H, \) Dyn, max Pdis
- \( 125C<Tj<150C, 1000 H, \) Dyn, max Pdis
- \( 150<Tj<175C, 500 H, \) Dyn, max Pdis
- \( Ta=125C, 120H, \) max Pdis
Low Temperature Operating Life Test

- Determine the reliability of devices under low temperature conditions over an extended period of time.
- Check for hot carrier effects, a commonly encountered failure mechanism accelerated by high voltage and low temperature.

Test Conditions:
- Maximum temperature: -10 deg C
- Electrical testing must be performed within 96 hours after the bias to the device has been removed.
High Temperature Storage Test

- Determine the effect on devices of long-term storage at elevated temperatures without any electrical stresses applied.

- The purpose is to assess the long-term reliability of devices under high temperature conditions.

Summary of industry-standard HTS conditions: 1000 hours at 150 deg C.
Mil Std 883, Method 1008, Stabilization Bake Specs:

- storage at a high temperature for a specified duration
- Test Condition A: 75 deg C / 24 hours minimum
- Test Condition B: 125 deg C / 24 hours minimum
- Test Condition C: 150 deg C / 24 hours minimum
- Test Condition D: 200 deg C / 24 hours minimum
- Test Condition E: 250 deg C / 24 hours minimum
- Test Condition F: 300 deg C / 24 hours minimum
- Test Condition G: 350 deg C / 24 hours minimum
- Test Condition H: 400 deg C / 24 hours minimum
Thank You!